A Low-power CMOS Pull-up Circuit

Reza Taherkhani, Ali Heidary, Guijie Wang and Gerard C. M. Meijer

Abstract – **In this paper, a low-power internal pull-up circuit is *presented*. For power management, many chips are implemented with a power-down (PD) pin. This paper describes a nonlinear circuit which can pull-up the PD pin through a low-ohmic path, which in default circumstances drives the pin voltage into the ON state with a high immunity for the effects of interference. This opens the option to control the PD pin externally or to use it floating. In both cases the circuit consumes only very little current. The circuit is implemented in 0.7µm CMOS technology with our smart temperature sensor. The simulation results which is in close agreement with our measurement results, shows that for the supply range of 2.7V to 5.5V in the temperature range of -45ºC to 130ºC and for all different corners of technology, the current consumption in power-down mode is less than 2µA, while the pull-up impedance is less than 50 kΩ. The measured power down current in room temperature, which is in very close agreement with simulation results is less than 1µA for all range of supply voltage. Also the measured pull up resistor for 3.3V supply at room temperature is about 26kΩ.**

Keywords –**Low power, Power management, Power down**

I. INTRODUCTION

For power management, many chips have a power-down (PD) pin, which is externally controlled. For instance, with a HIGH voltage the chip functions properly, while for a LOW voltage is in the PD mode. For a specific group of chip users, which don't need the PD option, but prefer to have a minimum number of pins, it would be desirable that in case of a floating PD pin the chip is automatically driven into the ON state. This can be achieved with an internal pull-up resistor. For immunity for interference, it will be required that the impedance of such a resistor is sufficiently low, which has the drawback that it significantly increases the current consumption for users who do use the PD option of the same chip. To solve this problem, we designed a nonlinear power-up circuit which drives a floating pin into the HIGH state and yet has a low input impedance, while in the HIGH, or FLOATING state consume no current, its current in LOW state is also very low. This circuit is applied in a smart temperature sensor [1] that optionally can be used in packages with three pins only (same as existing chip [2]), without PD option. With such an internal pull up circuit, the power down pin can left unwired. While in other applications, the same chip can be used in packages with four pins, including a PD pin.

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II. PROPOSED CIRCUIT

A very common, but not power-efficient, pull-up circuit consists of just a pull-up resistor *R* (Fig.1 (a)). With a 5V supply, limitation of the current in the power-down mode to, for instance, 5µA would require that *R*> 1MΩ. Such a high resistance would make the input circuit rather sensitive for interference. This shows that for low-power application it would be desirable to use a non-linear pull-up resistor, which offers a low resistance in the power-up state with floating PD pin, and a low current consumption in an externally-controlled PD state. This concept shows some similarity to that of open-drain signal busses using pull-up resistor (Fig.1 (b)). Selection of the resistor value poses the problem that with a small resistor the pull-down current is large, while with a large resistor the rise time will be large. One solution to this problem is to make a nonlinear resistor by switching [3] or in a more advanced way [4].

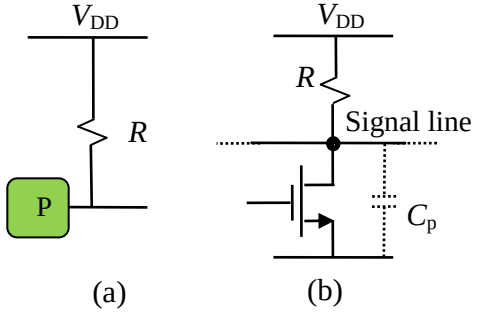

Fig. 1. (a) Resistor power-up circuit; (b) Resistor pull-up circuit for open collector signal line.

Figure 2 shows the proposed low-current power-up circuit for the PD pin. Node PD_i is a chip pin which may be connected to a package pin or can be left floating. In principal this node can also be used to power-down the chip circuitry. However, in that case the parasitic capacitor at node PD_i will be larger. As will be described below, this makes power up slower. Instead, we use the output of node PD_o, which has the same logic level as node PD_i, as power-down control signal.

To understand the behavior of the circuit depicted in Fig. 2, we first suppose that input pin PD_i is floating (not connected) and the power supply is just turned on. Furthermore, we suppose that the parasitic capacitor C_p at node PD_i has no charge and that the voltage V_{PDi} at this node is zero. Then, transistor M2 is conductive, so that the voltages at nodes A and PD_o are V_{dd} and *'0'*, respectively. With this condition, transistor M_3 is turned OFF, and the

only current that charges parasitic capacitor C_p is the drain current I_{d6} of transistors M_6.

In the LOW state of node PD_o, as long as the voltage V_{PDi} is lower than the PMOS threshold voltage $|V_{TP}|$, transistor M_6 is in saturation. When transistors M_6 and M_7 have the same size, and when we ignore the body effect, then it can be shown that the charging current of C_p amounts to about:

$$I_{d6} = \frac{\mu_p C_{ox} W_7}{2L_7}\left(V_{dd}/2 - |V_{Tp}|\right)^2, \qquad (1)$$

where, μ_p, C_{ox}, W and L represent the mobility of holes in the channel, the gate-oxide capacitance per unit area, channel width, and channel length, respectively.

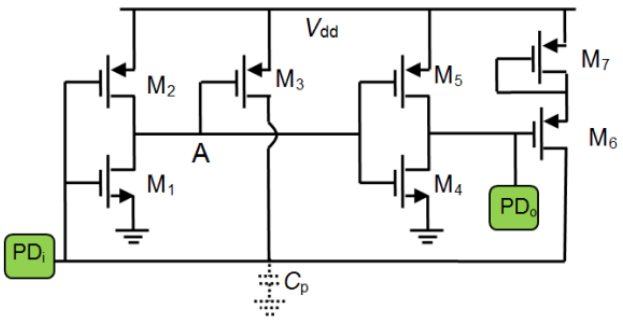

Fig. 2. Proposed power-up circuit

The first inverter M_1 and M_2 has been designed in such a way that, before the voltage at node PD_i, reaches the value $|V_{TP}|$ (before M_6 goes into ohmic region), its output switch to low state and turns on the transistor M_3. This can be set by selecting $W_1/L_1 >> W_2/L_2$. After this transition, the voltage at node PD_o goes to the HIGH state and turns off transistors M_6 and M_7, which are not needed anymore, while transistor M_3 completes charging of C_p, with a much larger current. When V_{PDi} approaches V_{dd}, transistor M_3 is driven into its ohmic region. Its channel resistor R_{DS} equals the input resistance R_{PDiH} for the HIGH state of input pin PD_i, and amounts to:

$$R_{PDiH}{}^{-1} = \frac{\mu_p C_{ox} W_3}{L_3}\left(V_{dd} - |V_{Tp}|\right), \qquad (3)$$

By appropriate selection of W_3/L_3, the required equivalent pull-up resistor for HIGH state R_{PDiH} can be set.

As can be realized, the equivalent pull-up resistor for HIGH state is set by M_3, while the current consumption in PD mode (LOW state) is set by M_6 and M_7 which can make the design of this circuit very flexible: Using small transistor for M_6 and M_7 will guarantee that the current in the (externally-controlled) PD mode is low. While the use of a larger transistor for M_3 guarantees that with a floating PD_i pin and as soon as the voltage is pulled up to the HIGH state, this pin is connected with a low-impedance R_{PDiH} to V_{dd}.

III. Simulation and Measurement Results

The proposed circuit was implemented in 0.7µm standards CMOS technology. As mentioned before, this circuit is used in smart temperature sensors, which should work with supply voltages ranging from 2.7V to 5.5V (with a typical value of 3.3V), and a temperature range of -45ºC to 130ºC. We designed the pull-up circuit to have a current consumption of less than 1µA for whole range of supply and an equivalent pull-up resistor of about 25 kΩ for V_{dd} =3.3V, T=300ºK. Another point of interest was the minimum available current for charging parasitic capacitor C_p. In case of a floating condition of the PD_i pin, this current should be large enough to guarantee a rapid ramp up of V_{PDi}.

To meet our specification the sizes of the transistors have been selected as:

$$\frac{W_6}{L_6} = \frac{W_7}{L_7} = \frac{2\mu m}{40\mu m} \;\&\; \frac{W_3}{L_3} = \frac{2\mu m}{2\mu m}\&$$

$$\frac{W_1}{L_1} = \frac{30\mu m}{0.7\mu m} \;\&\; \frac{W_2}{L_2} = \frac{2\mu m}{2\mu m} \;\&\; \frac{W_4}{L_4} = \frac{2\mu m}{0.7\mu m} \;\&\; \frac{W_5}{L_5} = \frac{6\mu m}{0.7\mu m}.$$

Figure 3 shows the simulated and also measured quasi static I-V characteristic of the input PD_i for V_{DD}=3.3V at room temperature. The simulations has been performed in Cadence software with typical transistor parameters along with worse case corners. It should be mentioned that the two inverters (Fig. 2) only consume some current during the transition of the voltage V_{PDi} during powering up. As can be realized the measured value is in very close agreement with predicted value in the simulator. With external control of pin PD_i, when V_{PDi} is LOW, the measured current has a very low value of about 80nA. With a floating pin PD_i, in the steady-state condition, this pin is strongly connected to V_{DD}. The equivalent resistor in this state is equals to the slope of the curve in Fig. 3 for V_{PDi}= 3.3V and its measured value amounts to about 26 kΩ.

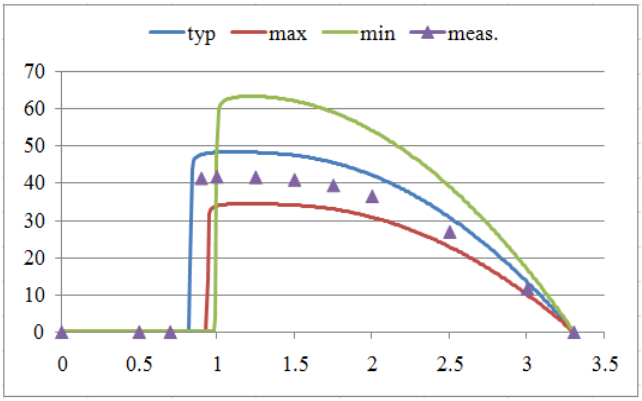

Fig. 3. The simulated and measured I-V characteristic at pin PDi for VDD=3.3V and T=300ºK.

Figure 4 shows the measured and simulated supply current in low state (PD state) versus supply voltage at room temperature. The simulation result is for typical transistor parameter and also for worse case corners. The maximum simulated current is about 1.6µA and the minimum is about 2 nA. The minimum current is much larger than any possible leakage current at node PD_i and will charge the parasitic capacitance at this node with sufficient speed. The measured results in this case are also very close to simulation results. It should be mentioned here that, our temperature sensor consume about 60µA. Therefore the power down current of about 1µA is small enough.

To find the range of charging current in low state and also the maximum pull-up resistance in the HIGH state R_{PDiH} we need to consider all corner including supply and temperature range. The minimum charging current will happen at minimum supply voltage, 2.7V at -45C and amounts to 0.2nA. While the maximum pull down current is less than 2A which happens at maximum supply voltage, 2.7V at -45C .Also the maximum pull up resistance will occur for the smallest supply voltage of 2.7V at 130C which amounts to about 50kΩ.

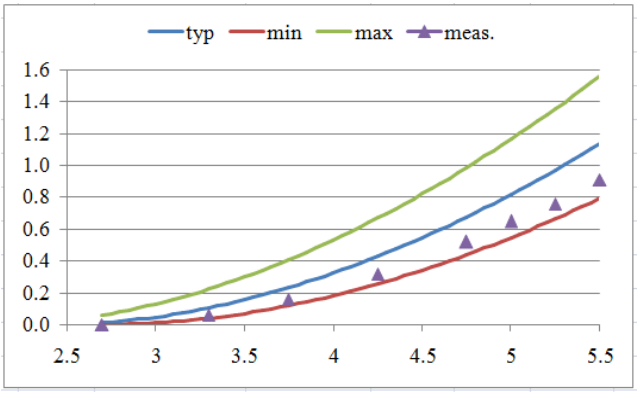

Fig. 4. Supply current versus supply voltage for different corners of technology at room temperature for LOW state (VPDi= 0) along with measured value for the same condition.

IV. CONCLUSION

A nonlinear pull-up circuit for power down pin (PD) is designed that for floating input conditions connects the PD pin to the high voltage through low-ohmic path with a resistance of about 25 kΩ for V_{DD} = 3.3 V. However, when PD pin is externally connected to ground, the power-up circuit consumes less than 0.1μA.

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