Fully Integrated Low Power Temperature Measurement Circuit Design in 28nm Process

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Abstract – **This paper presents a new on-die temperature detection principle and its circuit implementation in a 28 nm CMOS process. The suggested fully integrated circuit is capable of converting IC temperature to voltage in a range of -40°C to 125°C. Compared to conventional methods of temperature sensing the suggested solution is process and supply voltage independent. The circuit provides means for easy control of output voltage range depending on application specifics, consumes less than 1.4 mW power and requires about an 800 um^2 chip area. The principle theory, circuit implementation, simulation results and their correlation with theoretical values are discussed.**

Keywords – **Temperature measurement, PVT compensation, logarithmic amplifier, on-die temperature, temperature detection**

I. INTRODUCTION

Rapidly growing level of integration and data rates result in significant IC core temperature variations and gradients during system operation [1-3]. Temperature variation seriously affects such parameters of modern IC elements as transistor threshold voltage, effective impedance as well as integrated resistor resistance and as a result can significantly degrade circuit performance. This becomes more and more critical as SoC operating frequencies increase resulting in lower timing budget margins and technology processes becoming more susceptible to PVT variations. In I/O circuits the temperature variation degrades output and input impedance affecting signal matching in transmission lines, hence negatively impacting signal integrity and timing parameters [4, 5]. Most modern SoC components employ integrated calibration mechanisms to allow tuning of crucial components back to specified parameters. Examples of such systems are such high speed I/O standards as USB and DDR [4] where output and input impedances are periodically calibrated to minimize PVT variation effects [5, 6]. Some state of the art standards like DDR4 [4] allow for background mode (online) tuning to compensate for temperature changes during circuit operation. The above mentioned reasons as well as number of other applications [2, 3] create demand for SoC compatible temperature sensors. External sensors

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and thermo-pair based sensors have a number of disadvantages such as measurement error due to temperature difference in IC core and package as well as additional manufacturing/production cost. There are number of solutions for integrated sensors including BJT current measurement and ring oscillator based ones [2, 3], however they usually share such disadvantages as high variability with process and voltage. Namely ring oscillator frequency will drift substantially with process variation, obscuring frequency drift due to temperature, hence making the measurement less correct. The process variation effects cannot be neglected for technologies below 90 nm. This paper suggests a principally new, fully integrated solution based on modified logarithmic amplifier pair output voltage difference amplification. Compared to existing integrated solutions the presented circuit is highly tolerant to technology and supply voltage variations, has comparatively small area and low power consumption. The theory, measurement results and their correlation are presented.

II. TEMPERATURE DETECTION SUGGESTED PRINCIPLE

The principle of temperature detection is based on measuring the difference between two logarithmic amplifiers with a shared voltage bias and load resistance parameters, Fig.1.
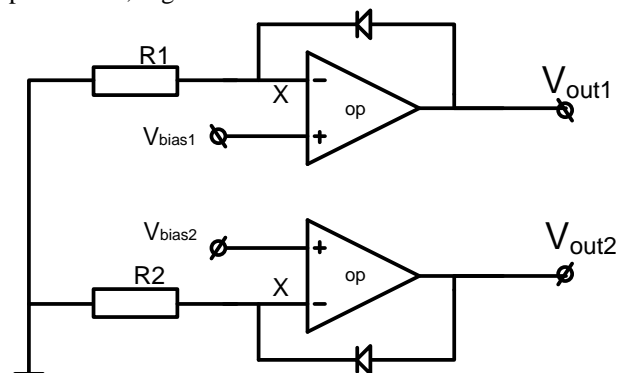

Fig. 1. Detection and sensing circuit principle

The bias voltage is generated internally and can be implemented by a simple resistive divider. The circuit can operate in two modes, when $V_{bias1}=V_{bias2}=V_{bias}$ (common bias mode), and when $V_{bias2}=m_b V_{bias1}$ (scaled bias mode, m_b is the bias scaling factor). Both current branches in Fig.1 have identical, preferably matched diodes. The resistors use identical structures with a different nominal value, achieved by a scaled number of parallel connected fingers. Poly-resistors available in all modern technology processes

can be used. Both branches are required to use the same single ended operational amplifier with shared bias current generators and properly matched critical elements. In common bias mode, the opamp negative inputs will be forced to V_{bias}, hence using diode current expression it can be easily shown that:

$$V_{out1} = V_{bias} + V_T \cdot ln\frac{V_{bias}}{R \cdot I_0} \quad (1)$$

The circuit branches separately behave like classic logarithmic circuits. If $R_2 = m_r R_1$ a similar expression for V_{out2}, after simple transformations can be rewritten respectively as follows:

$$V_{out2} = V_{bias} + V_T \cdot ln\frac{1}{m_r} + V_T \cdot ln\frac{V_{bias}}{R \cdot I_0} \quad (2)$$

Substituting Eq.1 into Eq.2 for Vout2 and Vout1 voltage difference the following expression can be shown:

$$V_{out2} - V_{out1} = V_T \cdot ln\frac{1}{m_r} = T \cdot \frac{k}{q} \cdot ln\frac{1}{m_r} \quad (3)$$

Hence, the output voltage difference after differential amplification by A, (V_{det}) will be described as:

$$V_{det} = A \cdot V_T \cdot ln\frac{1}{m_r} \quad (4)$$

As it can be seen from Eq.4 the detected voltage is strictly proportional to temperature and has no dependence on other factors such as operating voltage, logarithmic amplifier bias voltage and process corner. The parameters A and m_r serve as detected voltage scaling factors, which can be defined for a specific application. The Eq.1 and Eq.2 suggest that the same principle can be realized with a slightly different modification of the presented circuit, using the same load resistor value for both branches but different bias voltage values ($V_{bias2} = m_b V_{bias1} = m_b V_{bias}$) in Fig.1. For this case the expression (3) will be rewritten the following way:

$$V_{out2} - V_{out1} = (m_b - 1) \cdot V_{bias} + T \cdot \frac{k}{q} \cdot ln(m_b) \quad (6)$$

The resistor scaling can be used along with bias voltage scaling in order to increase the detected voltage range:

$$V_{out2} - V_{out1} = (m_b - 1) \cdot V_{bias} + T \cdot \frac{k}{q} ln(\frac{m_b}{m_r}) \quad (7)$$

The introduction of bias voltage scaling can be used to center the detected voltage range around a specific DC offset value.

III. TEMPERATURE DETECTION CIRCUIT DESCRIPTION

The temperature detection system consists of the logarithmic amplification pair with sensing diodes, controlled gain differential to single amplifier, bias generation and control blocks, Fig.2. The control block implements basic digital logic and performs signal conditioning to control the bias generator operation mode, dual to single amplifier gain and allows to put the circuit into power down when detection is not required. The logarithmic amplification pair functions as a main temperature sensing block. It is implemented by the principle described in previous chapter, and consists of two identical operation amplifiers, two sensing diodes and a pair of resistors, Fig.1. The sensing diodes in this paper were implemented as forward biased drain-bulk diodes of PMOS devices. This solution can be preferred to conventional diodes or BJT devices for its considerably smaller area and better layout matching.
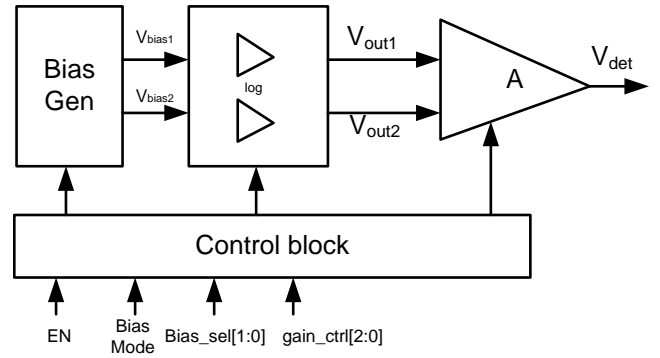

Fig. 2. Detection circuit block diagram

The behavior of the detection block is described by Eq.7. It can operate both in common and scaled bias voltage modes. In common bias mode the coefficient m_b equals to one hence the circuit outputs being described by expression (3). Different values of the aforementioned coefficient determine the detection voltage DC offset and range. The bias generator block (Fig.3) allows choosing between four m_b values, including the common bias mode.

It is activated by the control signal "ENn" and put into power down when the latter is de-asserted. In power down both the bias voltages are 0. The bias generator uses resistive dividers to generate bias voltage values. V_{bias1} is controlled by the "bias_sel[1:0]" signal, and connects it to the respective output of the resistive divider through analog multiplexor. When bias_sel[1:0]=2b'0 and/or bias_mode=1 V_{bias2} and V_{bias1} voltages are shunted together through the multiplexor and additional pass-gate putting the circuit into common bias voltage mode. The control block logic is implemented in a way that when bias_mode=1 then bias_sel[1:0] is asserted 0, so the circuit is forced to common bias mode, table 1.
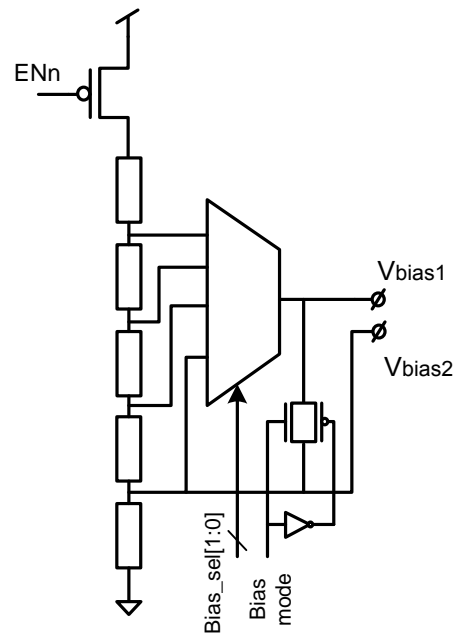

Fig. 3. Bias generation block

TABLE 1.   BIAS GENERATOR MODES

ENn	Bias_mode	Bias_sel[1:0]	m_b
1	-	-	Power-down
0	0	0	1
0	0	1	2
0	0	2	3
0	0	3	4
0	1	-	1

The dual to single amplifier (Fig.4) is a modified instrumentation amplifier. The choice of this topology in this paper is attributed to the fact that these amplifiers are known for low offset and robustness.
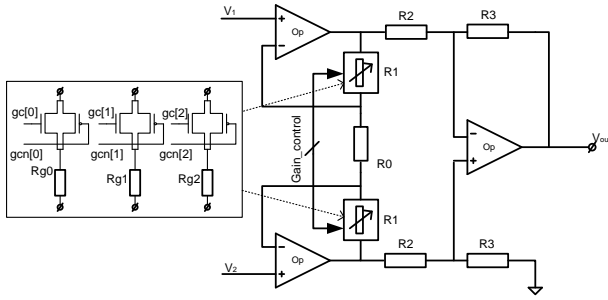

Fig. 4. Dual to single modified instrumentation amplifier

The amplifier gain is known to be described by following relationship:

$$A = \left(1 + \frac{2 \cdot R1}{R0}\right) \cdot \frac{R3}{R2} \quad (8)$$

The effective detected voltage for general and common bias modes will be described respectively as:

$$V_{det} = A \cdot (m_b - 1) \cdot V_{bias} + A \cdot T \cdot \frac{k}{q} \ln\left(\frac{m_b}{m_r}\right) \quad (9)$$

$$V_{det} = A \cdot T \cdot \frac{k}{q} \ln\left(\frac{1}{m_r}\right) \quad (10)$$

In this paper the conventional amplifier was modified to obtain gain control allowing for detected voltage range additional control. On the circuit level this is achieved using controlled impedance matrices for the R1 resistor, Fig. 4. The pass gate input signals are related to control block gain_ctrl[2:0] inputs with simple digital logic. The pass gate transistors are sized to have significantly less impedance than the resistors Rg0, Rg1 and Rg2, which eventually determine the gain. The designed amplifier has gain options equal to 1, 3 and 5. The nominal gain as well as controlled gain value number can be modified depending on specific design requirements.

IV. DESIGN AND SIMULATION SETUP

The proposed system was designed and implemented for a 28 nm CMOS process, with 0.9 V core device and 1.8 V thick-gate nominal voltages.

The schematic/physical design has been performed using the Synopsys Custom Designer tool. Global corner and Monte-Carlo simulations [7] were performed using Synopsys Hspice[7] and Finesim analog simulators. For graph plotting and numerical measurements Synopsys Cosmosscope tool was used.

V. SIMULATION RESULTS AND DISCUSSION

For global corner simulations the following cases were considered SS, TT, FF, FS and SF, with ±10 % of nominal supply voltage variations. The temperature detection circuit was simulated for -40°C to 125°C temperature range. Fig.5 shows DC sweep simulation results for the common bias operation mode. The considered circuit had the resistor scaling factor m_r=1/12 and dual to single amplifier gain was set to 3. The mentioned plot shows detector circuit voltage dependence on temperature in range of -40°C to125°C for SS minimal voltage, TT typical voltage and FF maximal voltage PVT corners. The dashed line corresponds to ideal dependence following from expression (10). The simulated voltage values show less than 3 mV deviation from theoretical value. As the formula (10) suggests the detected voltage is expected to have no dependence in supply voltage or process corner. This behavior is confirmed by simulations. The zoomed segment on Fig.5 suggests that detected voltage difference between slow and fast corners is less than 0.1 mV. The detected voltage is 196.6 mV at room temperature with range of 152 mV to 260 mV for -40°C to 125°C temperature range. The detected voltage can be stored or processed after analog to digital conversion. A 6 bit digital conversion will yield ~2.5°C per bit temperature detection resolution.
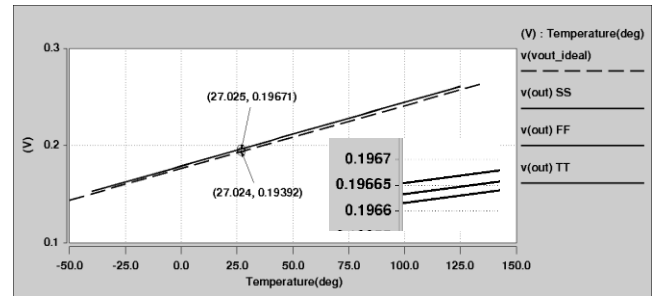

Fig. 5. Detector output voltage dependence on temperature, common bias mode

In some cases it may be preferred to have wider control over detection range and detected voltage DC offset, then scaled bias detection mode can be used. The voltage offset will be determined by m_b bias voltage scaling factor, as follows from (9). Fig.6 simulation plot shows detection voltage for 3 PVT corners when m_r=1/4, m_b=3 and A=3. As the theoretical expression and simulation results suggest the circuit output voltage offset will be dependent on supply variations. This can be useful when the analog to digital convertor is connected to the same supply, cancelling the detected value degradation due to ADC supply variations. The detected voltage at room temperature for slow, typical and fast cases is respectively 790 mV, 856 mV and 922 mV. Detection range is identical to the previous case. The presented circuit has practically no dependence on process corner and in case of common bias mode on supply voltage as well. Due to its symmetrical and fully differential structure the offsets of detection pair operational amplifiers cancel each other thus having no effect on detected voltage value. The sensing diodes can introduce detection error if not properly

matched. Fig.7 shows 3σ, 100 run Monte-Carlo simulation results for the common bias mode at typical simulation corner. The statistical simulation has shown 3σ = 2.2 mV for the detected voltage, which in case of 6 bit conversion is less than 1 bit error. The proposed circuit consumes 1.37 mW maximal power in fast PVT corner and requires around 800 um^2 silicon area with PMOS devices used for sensing diodes.
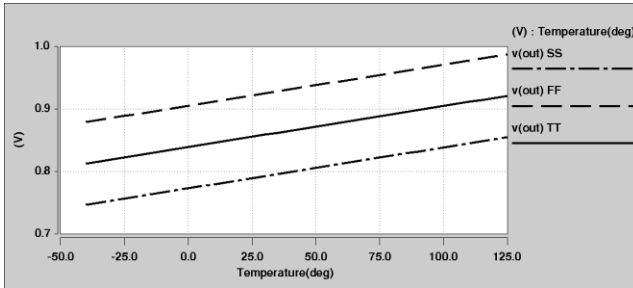

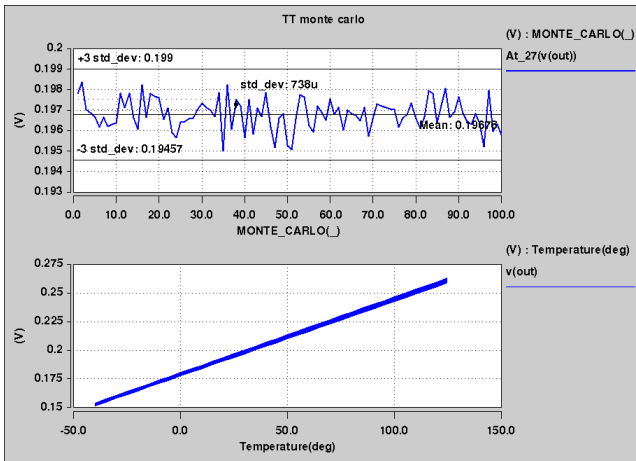Fig. 6. Detector output voltage dependence on temperature, scaled bias mode

Fig. 7. Statistical simulation results in common bias mode

The summary for the simulation results is presented in the table 2.

TABLE 2.   TEMPERATURE DETECTOR SUMMARY RESULTS

	Common bias mode			Scaled Bias mode		
	-40^{0}C	25^{0}C	125^{0}C	-40^{0}C	25^{0}C	125^{0}C
V$_{det}$; SS min. voltage (mV)	152.8	196.59	260.09	746	790	855
V$_{det}$; TT nom. voltage (mV)	152.81	196.6	260.1	812	856	920
V$_{det}$; FF max. voltage (mV)	152.82	196.62	260.12	878	922	0.99
Theoretical target value	150.4	194	257	-	-	-

Output voltage range (mV)	108	107
Monte carlo σV$_{det}$ (mV)	0.738	0.788
Max power; FF max. voltage **(mW)**	1.31	1.37

As demonstrated in the simulation results, the detected voltage in common bias mode has very high tolerance to process and voltage conditions yielding stable absolute voltage. The scaled bias mode allows the output voltage to drift in line with supply voltage, which can be practical in cases when analog to digital conversion is performed from the same supply. The detected voltage values and range can be easily tuned for a specific application since the detection circuit simulation values are in precise correlation (less than 2% deviation) with presented theoretical expressions.

VI. CONCLUSION

A principally new temperature detention method and its circuit implementation in 28 nm CMOS technology are presented. The principle is based on differential amplification of logarithmic amplifier outputs under scaled bias conditions. The designed circuit is fully integrated, uses no external components and requires about 800 um^2 of on-die area and less than 1.4 mW maximal power consumption. The theory of the suggested method is presented and compared to simulation results. Simulations of temperature detection voltage have shown very good correlation with theoretically expected values for temperature range of -40°C to 125°C and practically no dependence on process and supply variation. The design allows for output voltage range and DC offset values to be easily adjusted for a specific application.

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