Design of High-efficiency Dual-ratio Step-down Switched Capacitor Converter with Full Digital Feedback Control

Vazgen Shavarsh Melikyan and Vache Ashot Galstyan

Abstract – **The paper presents a novel adaptive digital control technique for multi-topology step-down switched-capacitor (SC) converter. The control system performs dynamic frequency modulation depending on load current as well as adjusts the conversion ratio to provide the required output voltage level. A novel non-overlap clock generator (NOCG) used in feedback control provides adjustable non-overlap period for switch control signals and enables the implementation of soft charging technique which reduces the output voltage ripple to 5mV. Proposed converter achieves 40ns response time to 60mA load variations and average conversion efficiency of 89% over wide range of load currents. The converter is designed in 28nm CMOS process using the proposed technique.**

Keywords – **CMOS, power converter, pulse frequency modulation, digital control oscillator, non-overlap clock generator, output ripple, conversion efficiency.**

I. INTRODUCTION

SC converters are widely used in up-to-date low power portable electronic systems to provide independent voltage conversion which is required for per module power management [1]. Primary function of DC-DC SC converters is the conversion of DC voltage at the input terminals into another DC voltage at the output terminal [2]. SC converters consist of power stage, which is responsible for voltage conversion and feedback control, which assures overall efficiency, load and line regulation characteristics of the system. The power stage is a dual phase structure which contains flying capacitors, switches and an output capacitor connected in corresponding way to form the required topology [3]. During the charging phase (Ph1), flying capacitors are connected to the battery and charged to the appropriate voltage. During the discharge phase (Ph2), flying capacitors are connected to the output node and discharge into the load through the output capacitor, thus providing the required output voltage. The most popular control technique for SC power converter is the pulse frequency modulation (PFM), where the switching frequency of the switches increases with the increase of the load current. Primary characteristics of SC converters are the voltage-conversion ratio (VCR), and the conversion efficiency (η). VCR is defined as the ratio between output voltage V_{out} and the input voltage V_{in} (Eq. 1), while the efficiency is the ratio of the converter's output power and input power. The efficiency has an upper bound equal to the ratio of the actual VCR and the iVCR: ideal VCR (Eq. 2), which is the maximum possible ratio between the output and input voltages of the conversion block.

$$VCR = \frac{Vout}{Vin} \qquad (1)$$

$$\eta_{\max} = \frac{VCR}{iVCR} \qquad (2)$$

A certain topology of SC converter corresponds to a specified VCR, which is the main disadvantage of SC converters. In order to increase input/output voltage range a multi-topology configuration is developed. Main challenge for modern SC converter design is to maintain low level of output ripple while providing high conversion efficiency for wide range of loads.

V. Melikyan is with the Synopsys Armenia CJSC, 41 Arshakunyats Ave, 0026 Yerevan, Armenia, e-mail: vazgenm@synopsys.com
V. Galstyan is with the Synopsys Armenia CJSC, 41 Arshakunyats Ave, 0026 Yerevan, Armenia, e-mail: vache@synopsys.com

II. STRUCTURE OF THE POWER CELL

The power stage topology proposed for this application is a dual-ratio, eight switch design shown in Fig. 1. With 1.4V input voltage, nominal output voltages of 0.75, 0.5 can be obtained.

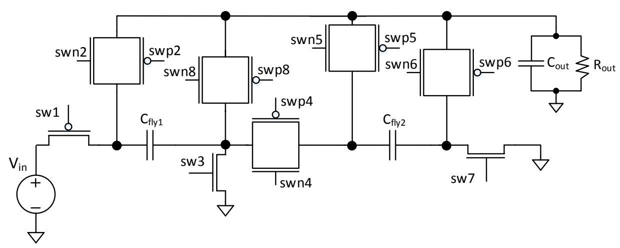

Fig. 1. Structure of the power cell

Switches connecting the input voltage source and flying capacitors were implemented with PMOS transistors which cover the whole operational range of the input voltage, while NMOS transistors where used to connect flying capacitors to the ground, thus lowering the area occupied by the switches. All remaining switches were implemented using transmission gates, i.e. NMOS and PMOS transistors connected in parallel which provided a low equivalent switch resistance. By varying how the switches are clocked, according to the TabSle I, conversion ratios of 1/2 and 1/3 can be obtained [5].

TABLE 1. SWITCH OPERATION FOR EACH PHASE AND MODE

Topology	Phase	Sw1	Sw2	Sw3	Sw4	Sw5	Sw6	Sw7	Sw8
1/2	**Ph1**	**ON**	**OFF**	**OFF**	**OFF**	**OFF**	**OFF**	**OFF**	ON
1/2	Ph2	OFF	ON	ON	OFF	OFF	OFF	OF	OFF
1/3	**Ph1**	**ON**	**OFF**	**OFF**	**ON**	**OFF**	**ON**	**OFF**	**OFF**
1/3	Ph2	OFF	ON	ON	OFF	ON	OFF	ON	OFF

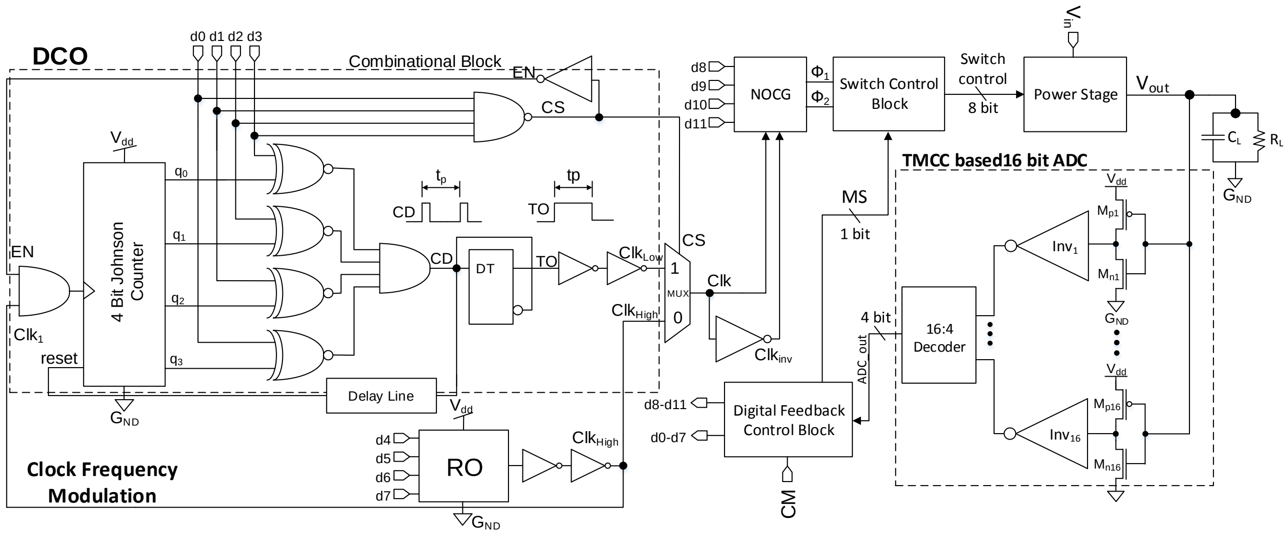

Fig. 2. System Architecture of proposed SC converter

III. SYSTEM ARCHITECTURE AND DESIGN STRATEGY

A novel digital control system is proposed which consists of threshold modified comparator circuit (TMCC) based analog-to-digital converter (ADC), digital control oscillator (DCO), NOCG and digital control block which adjusts the feedback system and power stage topology (Fig.2). Main goals for developing the feedback control were to eliminate the usage of reference voltages, as well as to assure fast load regulation response speed. The principle of PFM is shown in Fig. 3, which is the control of output voltage by modifying the switching frequency according to the load.

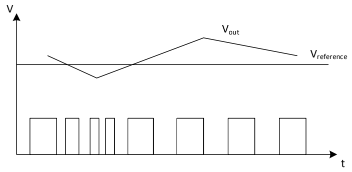

Fig. 3. Principle of frequency modulation

In order to track the output variations, conventional SC converters use a reference voltage and comparator circuit [4]. In proposed design a novel TMCC based 16 bit ADC is implemented which eliminates the usage of reference voltage and reduces the power consumption of the feedback circuit [5]. Unlike traditional Flash ADC, the series combination of resistors is replaced with TMCCs. TMCC is an inverter circuit with modified threshold voltage followed by NOT gate (Fig. 4). According to the required reference voltage, the threshold of corresponding inverter can be modified by modifying the width-length ratio of the MOSFETS (Eq.3).

$$V_{th} = \frac{V_{tn} + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}(V_{DD} - |V_{tp}|)}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}} \quad (3)$$

Then the input of the TMCC is less than the threshold, the output is interpreted as logic ‘1’. For input voltage higher than threshold, the output will be logic ‘0’. The extra NOT gates perform the function of logical restoration of inverter outputs. This approach ensures great decrease in power and area consumption as the bulky resistors are replaced by inverters and no constant shut through current is present from VDD to ground. The ADC output is then transferred to 16:4 decoder which is connected to the digital feedback control (DFC) block. DFC is a digital comparator, which performs adjustment of feedback circuitry according to ADC output code.

One bit Mode Select (MS) signal is used for selection between SC topologies with different conversion ratios. The logic ‘0’ and logic ‘1’ values for MS corresponds to 1/3 and 1/2 conversion ratios respectively.

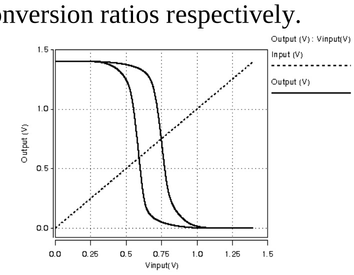

Fig. 4. Inverter threshold modulation

As the switched capacitor converters work with relatively low frequencies, a novel DCO circuit was proposed which consists of a digital control ring oscillator (RO), which generates the high frequency component of clock signal, and of a combinational block (CB) which uses the RO output to generate the low frequency component (Fig, 2).

Proposed RO is a 7 stage structure, where each stage consists of a 3 transistor XOR element and a transmission gate (Fig. 5). The delay of each stage is a summary of XOR and transmission (TG) gate delays which forms the output clock signal frequency. The delay of TG depends on the resistances of NMOS and PMOS transistors (Eq. 4) which are controlled by 4 bit digital code (Eq. 5). By manipulating the digital control, 16 fixed output clock frequencies can be obtained within output frequency range from 1.6GHz to 2.5GHz. The proposed DCO ensures up to 3 times less average power consumption than conventional analog VCOs.

$$t_{delay} = 0.7\,(R_n||R_p)C_{load} \quad (4)$$

$$R_{p,n} = \frac{VDD}{\frac{KP_{p,n}}{2} * \frac{(W_{p,n}+d0*W_{lp,n1}+\dots+d3*W_{lp,n4})}{L} * (VDD-V_{THp,n})^2} \quad (5)$$

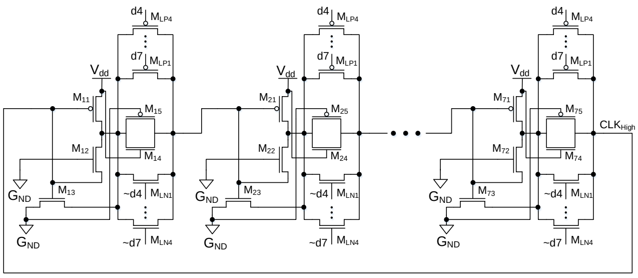

Fig. 5. Structure of Digital Control Ring Oscillator

The CB uses 4 bit Johnson counter and a digital comparator to generate the low-frequency clock signal. The CB output frequency is also controlled by 4 bit digital signal and varies from 120MHz to 1.2GHz. Hence, the output frequency range of proposed DCO is 2.38GHz. To provide similar frequency range with the usage of conventional ring oscillator, 40% more transistors must be used. With 8 bit overall frequency control, the proposed DCO provides acceptable frequency controllability while assuring less power consumption and transistor usage.

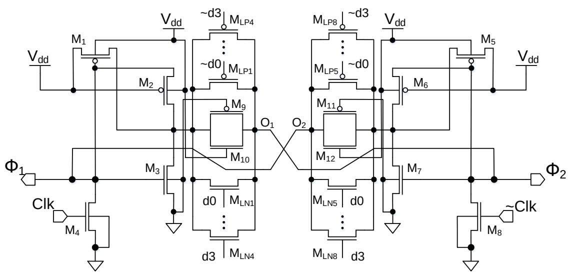

Fig. 6. Proposed non-overlap clock generator

The proposed NOCG (Fig. 6) is a back to back circuit which has similar structure as the RO stage [6]. By means of digital control code, both non-overlap period and rise/fall times of output two phase clock signal are controlled.

One of the major requirements for SC converter is the low output voltage ripple, which is the result of SC construction [7]. The current pulse on the flying capacitances decays gradually by RC time component, where R is the on-resistance of the switches and C is the flying or charge transfer capacitance. The difference between the current pulse and the load current is injected in the output capacitor, thus creating an output ripple (Eq. 6).

$$\Delta V = \frac{Q_{out}}{C_{Load}} \quad (6)$$

For heavy loading conditions with high switching frequency the output voltage ripple is relatively low. In order to have small output ripple for lights loads either the switching frequency must be increased or additional technique must be implemented. The increase of switching frequency will cause unreasonable leap of system power consumption. Hence the soft charging technique of flying capacitances is implemented with the usage of proposed NOCG which suggests opening the switch transistors gradually rather than in a step fashion. In this case the transistors' resistance is modulated such that the generated current on the flying capacitance matches the load current in each switching phase. Therefore no extra charge is injected in the output capacitance and the output ripple is be eliminated.

IV. Simulation Results

Proposed SC converted is designed using CMOS 28nm technology. Simulations where performed for input voltage equal to 1.4V. The clock signal generated by proposed digital control ring oscillator is shown in Fig. 7. The output frequency depends on the digital control code, and the pulse period varies from 392ps to 619ps.

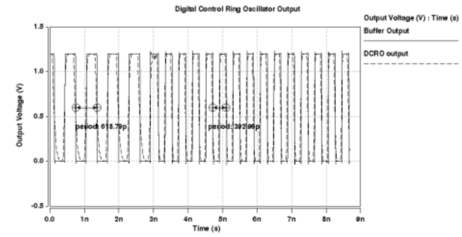

Fig. 7. High frequency output clock signal of RO

As shown in Fig. 8, output ripple at light load varies from 2.8mV to 5mV. At heavy loads converter operates at Fast Switching Limit (FSL) region with high switching frequency, therefore eliminating the output ripple at acceptable level of 5mV. For light loads because of soft charging technique the output ripple varies around 3mV.

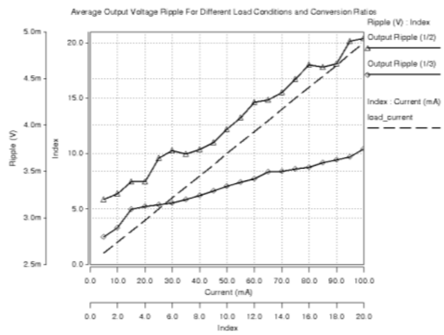

Fig. 8. Output ripple of the SC converter under different loading conditions

Fig. 9 shows the startup transient response of the converter which depends on the current topology of power cell. As it can be seen, the startup time for 1/2 topology is 70ns. Relatively slow startup time is caused by setup time of digital control circuitry of power cell.

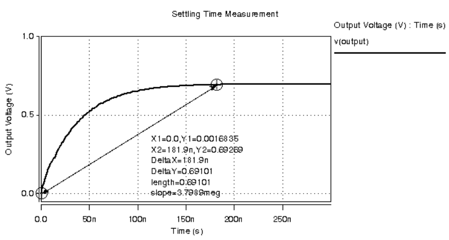

Fig. 9. Startup transient response

The usage of low power components and overall digital based feedback ensures high conversion efficiency over wide range of varying load conditions as shown in Fig.10.

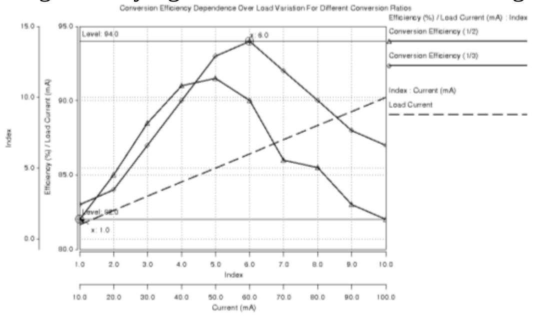

Fig. 10. Efficiency measurements of multi-topology converter at varying load conditions

Fig. 11 shows the transient response of the converter when load current is changed from 50mA to 10mA and the topology is switched from 1/3 to 1/2 and back. As shown in figure, the switching frequency is changed and the output voltage enters the permissible range during 70ns.

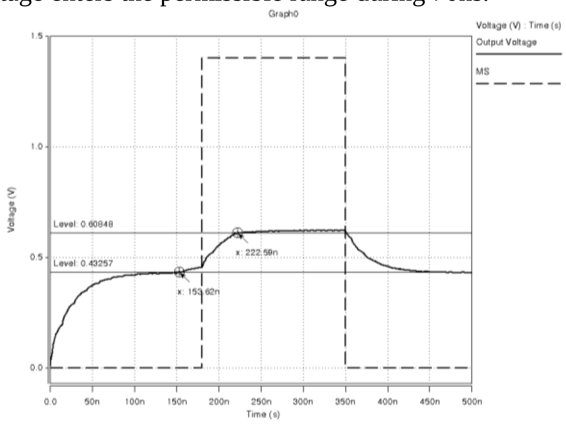

Fig. 11. SC converter transient response to load variation

Table 2 shows the performance comparison of proposed SC converter with similar designs [8] [9]. By means of the novel control methodology, the proposed design demonstrated the highest actual conversion efficiency, better startup and response characteristics as well as lower level of output voltage ripple.

TABLE 2. PERFORMANCE COMPARISON OF THE DESIGNED SC CONVERTER WITH SIMILAR DESIGNS IN THE LITERATURE

Parameter	Proposed Design	[8]	[9]
Voltage Conversion Ratio	1/2, 1/3	2/5	1/2, 1/3
Supply Voltage (V)	1.2 – 2.5	3.3	2.5V
Output Voltage (V)	0.4 – 1.25	1.25V	0.9-1.5
Theoretical max. Conversion Efficiency (%)	98	N/A	100
Average Conversion Efficiency (%)	89	64	50-66.7
Output Ripple (mV)	5	45	110
Cout (nF)	0.25	0.5	440
Cfly (nF)	0.8	3	6.72
Maximum output current (mA)	100	10.3	5
Maximal Switching Frequency (MHz)	200	40	1
Technology (nm CMOS)	28	18	0.35

V. CONCLUSION

A multi-topology SC converter with a novel control technique is proposed and the respective circuit designed. The usage of full digital control with low power components and dual ratio power cell configuration provided higher average conversion efficiency of 89% and lower output voltage ripple of 5mV compared with other designs. The other advantage of proposed circuit is the absence of reference voltage in feedback control circuit, which ensures easy integration and overall simplicity of usage. Main disadvantage of proposed converter is slightly slow start-up time and overall complexity of feedback control circuit.

ACKNOWLEDGMENTS

The research is supported by SCS MES RA, within the frames of joint Armenian - Belarusian research project № 13РБ-045.

REFERENCES

[1] Maity B., Mandal P. *A high performance switched capacitor-based dc-dc buck converter suitable for embedded power management applications*, IEEE Transactions on Circuits and Systems, pp. 1-5, 2011.
[2] V. Melikyan, V. Galstyan. *Design of low-ripple multi-topology step-down switched capacitor power converter with adaptive control system*, Design & Test Symposium (EWDTS), pp. 1-4, 2014.
[3] C. Wei-Chung, M. Da-Long, S. Yi-Ping, L. Yu-Huei. *A Wide Load Range and High Efficiency Switched-Capacitor DC-DC Converter With Pseudo-Clock Controlled Load Dependent Frequency*, IEEE Transactions on Circuits and Systems, pp. 911-921, 2014.
[4] H. Kwan, Ng C. D., So V. W. *Design and analysis of dual-mode digital-control step-up switched-capacitor power converter with pulse-skipping and numerically controlled oscillator-based frequency modulation*, IEEE Transactions on very large scale integration (VLSI) systems, vol. 21, pp. 2132-2140, 2013.
[5] A. Kar, A. Majumder, A. Mondal. *Design of ultra-low power flash ADC using TMCC & bit referenced encoder in 180nm technology*, VLSI Systems, Architecture, Technology and Applications (VLSI-SATA), pp. 1-6, 2015.
[6] V. Melikyan, V. Galstyan, N. Melikyan, A. Aleksanyan. *Adjustable Low-Power Non-overlap Clock Generator for Switched-Capacitor Circuits*, International Conference on Electrical and Computing Engineering, pp. 103-107, 2015.
[7] L. G. Salem, R. Jain. *A Novel Control Technique to Eliminate Output-Voltage-Ripple in Switched-Capacitor DC-DC Converters*, VLSI Systems, Architecture, Technology and Applications (VLSI-SATA), pp. 1-6, 2015.
[8] K. Bhattacharyya, P. Mandal. *A Low Voltage, Low Ripple, on Chip, Dual Switch-Capacitor Based Hybrid DC-DC Converter*, IEEE Transactions on Circuits and Systems, pp. 661-666, 2008.
[9] L. Su, D. Ma, A. Brokaw. *Design and analysis of monolitic step-down SC power converter with subthreshold DPWM control for self-powered wireless sensors*, IEEE Transactions on Circuits and Systems, pp. 280-290, 2010.