Computer Investigation of CMOS Operational Transconductance Amplifier (OTA) with Improved Linearity Implemented on AMS 0.35 µm Process

Atanas Tanev, Ivan Stefanov Uzunov, Sotir Ouzounov and Marin Hristov Hristov

Abstract – **Transistor circuit of a single stage fully differential OTA implemented on AMS 0.35 µm process is investigated with simulations. The focus of the investigation is the linearization of the output current and the operation of the common-mode feedback circuit (CMFB). Total harmonic distortion of less than 1% is targeted as criterion for linearity. Different linearization techniques and their circuit implementation are implemented and compared. The OTA frequency response is also simulated and commented.**

Keywords – **amplifiers, operational transconductance amplifier, non-linear distortions, common-mode feedback.**

I. INTRODUCTION

Operational transconductance amplifiers (OTA, G_m amplifiers) are widely used as basic building blocks in many analog circuits and systems like active filters, variable gain amplifiers, data converters, etc [1]-[5]. They have several attractive properties: wide tunability of their G_m; high speed; low noise; ability to work at low supply voltages. OTA based bandpass filters with center frequency below 1 Hz, as well filters at 300 MHz are reported in the literature [6],[7]. The variability of the specs for the versatile applications and continuously modified properties of the new technological processes are the main driving forces for intensive investigation of these amplifiers for more than 25 years [4].

Ideally, the OTA is a voltage controlled current source: infinite input and output impedances; output current proportional to the input voltage ($i_{out} = G_m v_{in}$); infinite wide frequency response; completely linear; no output noise. The real OTA is realized as single- or multi-stage fully differential circuit in the most implementations in integrated circuits (IC) due to the well known advantages of the differential circuits [1],[2]. Its basis is the classical cascode differential pair. Many enhancement have been introduces for improving different performance aspects. The problems, which must be solved by the designer, are versatile and depend on the application: achieving the desired G_m (less than 1 nA/V for very low frequency filters, hundreds mA/V for HF applications); G_m tuning in desired range; increasing the output impedance; extension of the frequency response; robust common mode implementation; small dependence from temperature, process and voltage variability; low output noise. However, in majority of applications, the basic problem in the transconductance amplifiers is their linearity. It is a inherent problem, caused by the nonlinear characteristics of the transistors (quadratic dependence of the drain current from the overdrive voltage in the case of CMOS) and the necessity of working with low supply voltages. Many efforts have been invested in transconductor linearization and the progress has been substantial: the first proposed OTAs had a maximum input voltage of 30 mV, while nowadays the achievable linear range is about 1 V at supply voltages significantly lower [4],[7].

Degeneration resistors placed in series with the sources of the differential pairs and creating negative feedback are the classical way for improving the linearity [8]. Its basic advantage is the simplicity. If g_m is the transconductance of the transistors in the pair and R_{deg} is the value of the degeneration resistors, then the third order nonlinear product in the output current is proportional to $1/(1+g_m R_{deg})^3$. On the other hand, G_m of the whole OTA is reduced $1+g_m R_{deg}$ times, and that much is increased the output noise [5]. Some improvement of the method is proposed in [7] where dynamic resistances, created by MOS transistors, are used instead of linear resistors.

The OTA core in the second linearization method consists of two differential pairs with parallel connected inputs and outputs, which are crossed and have the same dynamic loads. In the crossed outputs the output currents of the pairs are subtracted. The parameters of the differential pairs, basically transistor sizes and tail currents, must be chosen in a way ensuring canceling the nonlinear components and preserving the linear component in the output currents of the pairs. Both conditions require different differential pairs and keeping relatively strict relationships between the parameters of the pairs. This makes the method frequency limited and sensitive to the temperature, process and bias voltage variations, which is its main drawback.

Versions of this method are applied in many practical circuits [5],[6],[9]-[11]. Very small transconductances for ultra low-frequency filters are realized in the same way [6]. Another application is shown in [9], where small degeneration source resistors for better linearity are used also. A further development of this method is given in [5],[10]. Both papers describe complete OTAs, consisting of three identical OTAs. The individual OTAs are not

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compensated for linearity. One of them is used as main OTA in the complete circuit and the other two together with additional elements (some specific attenuators) separate the nonlinear components and subtract them from the output current. The identity of the individual OTAs makes this method insensitive to temperature, process and supply voltage variations and extends the frequency band of operation. A drawback of the method is increased complexity of the circuit.

There are also other approaches. One of them is based on using of basic differential pairs, working in triode or weak inversion region and biasing in different ways the source dc voltage of the pair [12],[13] to achieve linearized transfer characteristic. Yet another method uses adaptive biasing of the tail current of the differential pair, making it depending on the input signal [14]. The source dc voltage must be stabilized in this case too. Bulk driven differential pair is proposed in [15]. The linearity in the circuit there is improved also by additional amplifiers placed in feedback in each arm of the pair.

In this paper we investigatethe OTA proposed in [7]. It is attractive due to its high frequency of operation and simplicity. In this paper we have studied the porting of the circuit to a specific technology process in its optimization for THD of 1%. The THD is derived from the output current.

II. Circuit Description

The investigated CMOS OTA, as it is given in [7], is shown in Fig. 1. It consists of a single differential pair M_1 and M_2 having transistors M_7 and M_8 as dynamic load. The DC drain voltages are set by a CMFB circuit, which is a pseudo-differential amplifier, formed by M_{cf1}-M_{cf4}. Resistors R_s monitor the average of OTA drain voltages and feed it to the input of CMFB amplifier. It is compared there with the desired common-mode voltage V_{CM} and the difference signal, taken from the drain of M_{cf2}, is returned to the gates of M_7 and M_8.

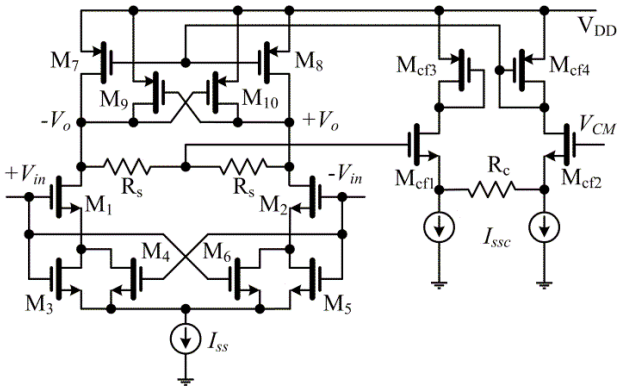

Fig. 1. Circuit of the investigated OTA.

Transistor pairs M_3-M_4 and M_5-M_6 form the degeneration resistors, linearizing the circuit. They operate in triode region and each transistor in the pair is controlled by a half of the input voltage with an opposite polarity. Thus, if the channel resistance of one of the transistors in the pair increases, the same resistance decreases in the other transistor. This reduces the unfavorable effect of the degeneration resistors on G_m of the OTA. The linearizing effect of the dynamic degeneration resistors depends on the ratio

$$a = \frac{\left(W/L\right)_{M1-2}}{\left(W/L\right)_{M3-6}} \quad (1)$$

where $a = 2$ is recommended in [7] as optimal for 0.13 μm process.

A negative resistance, formed by M_9 and M_{10}, is placed at the output for reducing the output conductance of the circuit. It is introduced due to the specific application of the circuit in [7] – for realizing high-Q bandpass active filters.

The simulations are done with AMS 0.35 μm CMOS process used in the education, which differs from 0.13 μm process in [7]. All transistor sizes are kept the same in the most of the simulations: $W = 10$ μm, $L = 0.35$ μm. They are the default sizes recommended for the process [16]. The value of the resistors R_s must be large and it is 100 kΩ, while the value of R_c is 1 kΩ. The tail current I_{ss} of the OTA is chosen to be 100 μA and the supply voltage is 3.3 V in all simulations.

III. CMFB and DC Bias

The goal of first simulation is determining of the currents I_{ssc} in the CMFB circuit. This circuit is a satellite circuit and it is important to reduce overall power consumption, by minimizing I_{ssc}. These simulations investigate the dependence of the output voltages (the voltage at "$-V_o$" node is chosen as representative) from I_{ssc}. OTA inputs "$+V_{in}$" and "$-V_{in}$" are connected to a 1.3 V dc voltage source. Fig. 2(a) shows the corresponding dependencies at three different voltages for V_{CM}: 1.25 V, 1.75 V and 2.25 V. The plots have two distinct parts: raising initial part, when the output voltages depend strongly from I_{ssc}; and a horizontal part, when this dependence is small and V_o is approximately equal to V_{CM}. The value of I_{ssc} should be at the beginning of the horizontal part – a minimum power consumption of the CMFB circuit is ensured in this way. The transition between both parts is at different value of I_{ssc} if the common-mode reference voltage V_{CM} varies. A conclusion from Fig. 2(a) is that $I_{ssc} = 25$ μA could be a good choice – it is the smallest value, which guaranties normal operation when V_{CM} increases up to 2.25 V. The effect of this choice will be examined also in the next simulations.

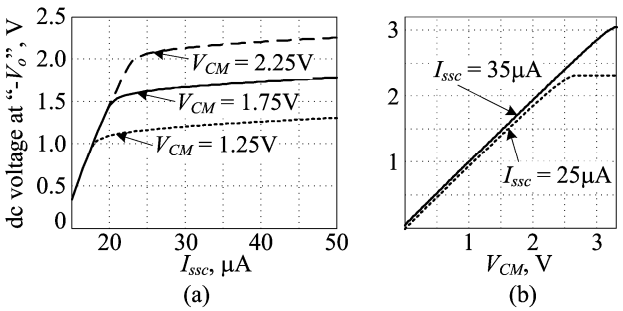

Fig. 2. Dependence of dc output voltage (at node "$-V_o$") from: (a) currents I_{ssc}; (b) common-mode reference voltage V_{CM}.

The plots from the next simulation, illustrating how dc output voltage is controlled by the common-mode reference voltage V_{CM}, is shown in Fig. 2(b). They confirm that 25 μA is the lowest boundary for I_{ssc}, since a horizontal part appears in the corresponding plot, when V_{CM} is above 2.5 V. This limitation does not exist in the plot at I_{ssc} = 35 μA – it demonstrates linear dependence of the output voltage from V_{CM} in the whole range from 0 to 3.3 V (V_{DD}).

The other simulations, which results are plotted in Fig. 3, investigate the changes of dc output voltage when some of the parameters of the basic differential pair vary. Fig. 3(a) shows that the output voltage does not depend on the common-mode input voltage (the plots are at I_{ssc} = 25 μA). The tail current I_{ss} affects the output voltage more significantly (Fig. 3(b)). There are again two areas in the plots: one with small dependence from I_{ss} and second, in which the output voltage rapidly drops down. These areas are visible in the plots for I_{ssc} = 25 μA and the boundary between them defines the upper limit for I_{ss}. This limit depends also from V_{CM} and it is between 110 and 130 μA for the considered plots. Upper limit for I_{ss} when I_{ssc} = 35 μA exists too but it is outside of the plotted area, i.e. the increased value of I_{ssc} increases also the robustness of the circuit versus variation of the tail current.

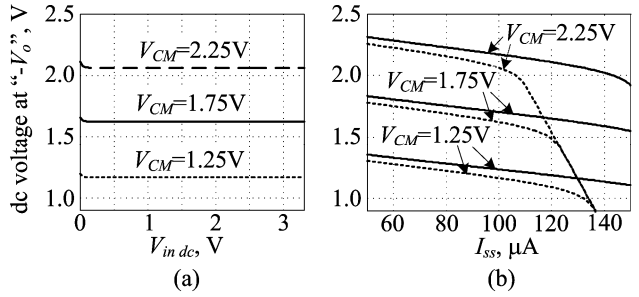

Fig. 3. Dependence of dc output voltage (at node "-V_o") from: (a) common-mode dc input voltage (at the gates of M_1 and M_2); (b) tail current I_{ss} (dotted lines are at I_{ssc} = 25 μA, continuous lines are at I_{ssc} = 35 μA).

The simulations in this section established the minimal values for the currents I_{ssc} in the CMFB amplifier, ensuring proper operation. They depend from few parameters: transistors dimensions, supply voltage, tail current in the basic differential pair, and upper limit for the common-mode reference voltage. Simulations, similar to the shown here, should be done for accurate determining of these currents in every specific case.

IV. Linearization of the Amplifier

The linearity of the amplifier and its dependence from the ratio *a*, defined by formula (1), is investigated briefly in [7]. The optimal value a = 2 is found by plotting G_m vs. differential input voltage at different values of *a*. Numerical criterion for linearity of the OTA itself is not presented in [7], instead are given measured data for IP3 of a G_m-C filter, realized by this OTA.

The OTA linearity is investigated here by using THD of the differential output current as a criterion. An AC voltage source with frequency of 1 kHz is placed at the input, and the output current is taken as the current through a capacitor with a large value (range of mF) connected between points "-V_o" and "+V_o" in Fig. 1 (short-circuited output). THD of 1% (-40 dB) is taken as conditional limit for linearity – the input voltage is increased until reaching this limit. This approach allows to evaluate the OTA linearity independently and to investigate its frequency dependence.

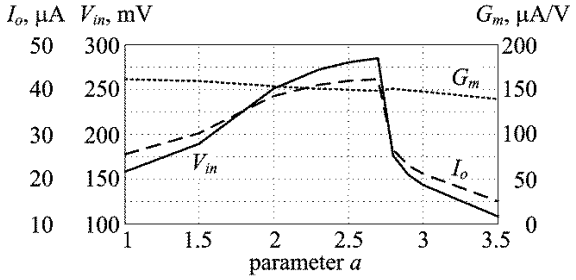

Fig. 4. The maximal undistorted amplitudes and G_m vs. parameter *a* from formula (1).

The first investigation is concerning the influence of the parameter *a* on the amplitudes of the input voltage V_{in} and output current I_o, at which is achieved the conditional limit for linearity (they can be considered as maximal undistorted amplitudes). The transistor sizes are as in the previous simulations and only the widths of M_1 and M_2 are varied for settling the desired value of *a*. The corresponding plots are shown in Fig. 4. The value of G_m is calculated as ratio between maximal undistorted amplitudes.

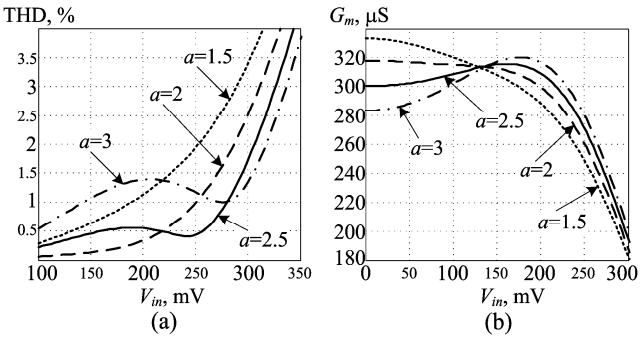

Fig. 5. (a) THD of the output current vs. amplitude of the input voltage; (b) G_m vs. amplitude of the input voltage.

The optimal value for *a*, which is seen in Fig. 4, is about 2.5 and it is different from the value given in [7]. Possible reasons for this difference could be difference in the processes, different transistor sizes, but the major is the different criteria for linearity. THD, chosen as criterion here, has interesting behavior, illustrated in Fig. 5(a). It has ripples when $a > 2$, which increase when *a* increases, but are still moderate if $a \leq 2.5$. These ripples extend the area where THD is less than 1%. This observation is confirmed by the plots of the differential G_m (= dI_{out}/dV_{in}) vs. amplitude V_{in}, shown in Fig 5(b). G_m has approximately flat behavior for lower values of *a* and it is in maximally wide area at a = 2. Above these value appear ripples, which increase with *a*. These ripples initially do not increase significantly the nonlinearity and the value of the parameter *a* can be optimized depending on the limit for the tolerated nonlinear distortion.

The simulation of maximal undistorted amplitudes and of G_m, done at a = 2.5, shows that they do not change significantly up to frequencies of 10 MHz (Fig. 6).

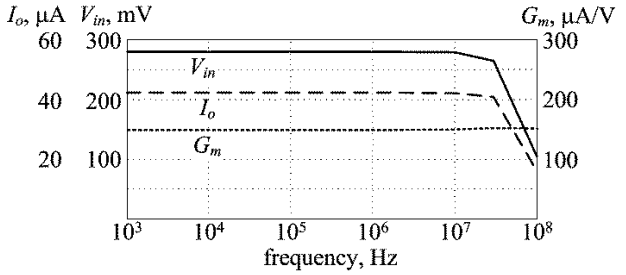

Fig. 6. Dependence of the maximal undistorted amplitudes and G_m from the frequency (a = 2.5).

V. Frequency Response

The frequency dependence of G_m in the OTA's is presented usually by one pole approximation [3]:

$$G_m = \frac{G_{m0}}{1+\left(s/\omega_c\right)}, \qquad (2)$$

where G_{m0} is the low-frequency value and ω_c is the -3 dB cut-off frequency. This approximation works for multi-stage amplifiers, but it cannot be used in the considered case.

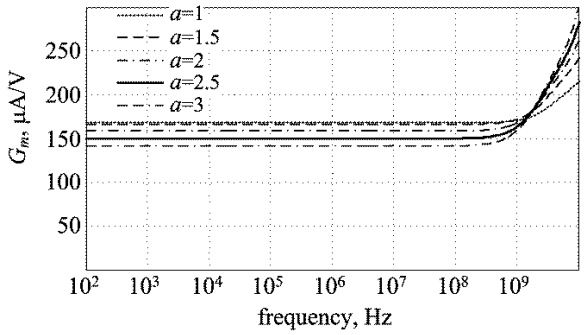

Fig. 7. Frequency dependence of G_m at different values of a.

Fig. 7 shows the frequency dependences of G_m at different values of the parameter a. All they are constant up to few hundreds of MHz and then start to raise. The increasing at very high frequencies is caused by the capacitances C_{gd} of M_1 and M_2. They connect directly the input with the output of the amplifier – point "+V_{in}" with "-V_o" and "-V_{in}" with "+V_o". These capacitances transfer a current, which increases with frequency, from the ideal voltage source at the input to the short circuiting capacitor at the output.

VI. Conclusion

The transistor level simulations, presented in this paper, analyzed the achievable linearity with a state-of-art OTA implementation, when using 350 nm AMS process. The paper studied the optimization of CMFB circuit power and the extension of the linear range of operation of the amplifier. A power consumption of 0.56 mW was achieved with 170 uA dc biasing current in the circuit.

The linearity is optimized by using of THD as a simple numerical criterion for linearity. A linear range of 270 mV for the amplitude of the input voltage was achieved. This approach allows easy to estimate the undistorted magnitudes of the input and output signals and also to determine the frequency limits of the considered linearization method.

The frequency response of the circuit is also investigated briefly. It is shown that the frequency dependence of G_m does not follow the one pole approximation given usually in the literature. This effect is caused by the parasitic gate-drain capacitances in the transistors in the differential pair.

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