Design Considerations for Current Mode Amplifier in Deep Sub-micron CMOS Technology

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Abstract – **A design procedure for current amplifier circuit, based on a combination of theoretical and graphical methods is proposed. Computer simulations demonstrate the good matching between specified and obtained circuit parameters. The linearity of the circuit and its frequency dependence is evaluated, using THD as criterion. Monte Carlo analysis is performed to estimate the parameter deviation due to process variations.**

Keywords – **Amplifiers, current amplifiers, CMOS, low input impedance, high output impedance.**

I. INTRODUCTION

Current mode operation in analog signal processing is undergoing extensive development in the past two decades, which is primarily driven by the permanent demand for supply voltage reduction [1,2]. Current mode circuits have several significant advantages [1-4]. They allow operation at much wider range of the signal levels compared to their voltage mode counterparts. They also have wider frequency bandwidth, better linearity, their circuits are simpler and usually consume less power.

Various types of current mode circuits are proposed in literature: operational transconductance amplifier, current conveyor, single ended current amplifier, current operational amplifier, current differencing amplifier, etc. They find application in many high performance analog and mixed signal processing blocks like sensor interfaces, data converters, filters, oscillators, and others.

The design of current amplifiers has some specifics in the modern CMOS technologies, creating serious challenges in the analog design. They are primarily related to device downscaling, where short channel effects become significant. These effects include channel length modulation, hot carrier injection, velocity saturation and drain-induced barrier lowering. As a result the device characteristics deviate from those of long channel FETs, e.g. the drain current is not a square law due to velocity saturation [4]. Those effects require modification of the existing design procedures and employment of new techniques based on computer simulation and optimization. An example of such approach is given in [5,6].

The methodology described in [5] is extended in this paper to design one of the most popular current mode amplifiers (Fig. 1), using a modern CMOS technology. This circuit serves as a basis for a family of current mode amplifiers with different properties: low input impedance [4], extended frequency bandwidth [4,7], current differencing amplifiers [3], input stage of a current operating amplifier [8]. The basic characteristics of the designed amplifier are investigated by simulation: dc operating point, frequency response, linearity, sensitivity about process variation.

The used process is 32nm bulk CMOS technology, developed for SRAM, logic and mixed-signal applications from IBM. Nominal operating voltage is 1V for thin gate oxide, but high voltage transistors with medium (1.5V and 1.8V) and thick gate oxide (2.5V and 3.3V) are available. Minimum drawn gate length is 30nm for thin oxide, and 270nm for thick oxide FETs.

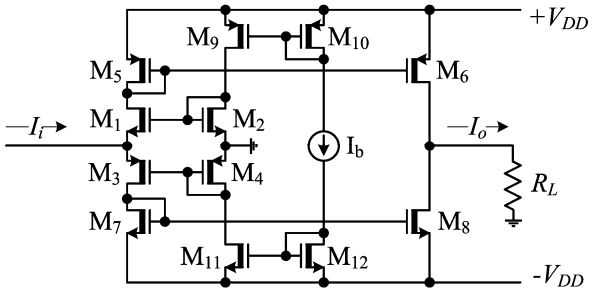

Fig. 1.The circuit of the basic current amplifier.

II. SHORT DESCRIPTION OF THE CIRCUIT

The operation of the circuit is based on several connected current mirrors. In quiescent point, the reference current I_b is copied through current mirrors M_{10}-M_9 and M_2-M_1 as a current through M_1. The same current is copied through M_3. Current mirrors M_5-M_6 and M_7-M_8 copy the identical currents through M_1 and M_3 as identical currents through M_6 and M_8 and the output current I_o is zero. When input current I_i is applied, it disbalances the currents in the upper (M_1 and M_5) and the lower (M_3 and M_7) parts of the input branch. This results as a proportional disbalance in the output branch and the difference between M_6 and M_8 drain currents flows through R_L as output current. The basic formulas for this amplifier are [3, 7, 9]:

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$$A_i = \frac{W_6/L_6}{W_5/L_5} = \frac{W_8/L_8}{W_7/L_7}\ ; \quad (1)$$

$$R_i = \frac{1}{g_{m1} + g_{mb1} + g_{m2} + g_{mb2}}\ ; \quad (2)$$

$$R_o = \frac{1}{g_{ds6} + g_{ds8}}\ , \quad (3)$$

where A_i is the current gain (output is short circuited), R_i is the input resistance, R_o is the output resistance, g_m's are the transconductances, g_{mb}'s are the back-gate transconductances and g_{ds}'s are the output conductances of the corresponding FETs.

III. Initial Design Centering

The design of the circuit, is in fact proper sizing of the devices to meet the specifications. The considerations here are focused on primary parameters: the gain, input and output impedances. The current gain is ensured simply by a proper choice of the aspect ratios of transistor pairs M_5—M_6 and M_7 – M_8 according to (1). The procedure to achieve the desired input impedance is more sophisticated. Mainly it depends on the transconductances of the input transistors M_1 and M_3, (equation (2)), but several factors cause difficulties: M_1 and M_3 are of different type – NMOS and PMOS, but g_m of the transistors should be kept equal to achieve symmetrical response for input signals with different polarity; the same current flows through both transistors; the back-gate transconductance should be taken into account.

The output impedance is defined by the output conductances of M_6 and M_8 (formula (3)). It is function of two parameters – the drain current and the channel length modulation parameter λ of these transistors according the well-known formula [2,9]

$$r_{ds} = \frac{1}{(I_{dsat}}\ . \quad (4)$$

The input and the output impedance depend on each other since: 1) the drain current of M_6 and M_8 is defined by the current through M_1 and M_3 multiplied by the current gain; 2) λ is process defined parameter. For this reason the output impedance will not be considered as design parameter here and the main focus will be on the input impedance and the symmetry of the input stage.

The bulks of the input transistors are not connected to their sources, which introduces g_{mb1} and g_{mb3} terms in formula (2). The back-gate transconductance usually is 10-20% of g_m [9]. This value can be refined by simulation of g_m and g_{mb} vs. V_{gs} shown in Fig. 2, where the back-gate effect is taken into account with V_{bs}=1.25V. The ratio g_{mb}/g_m obtained from the curves is 10-12%.

The design procedure will be illustrated by an example design of the basic current amplifier from Fig.1 with the following parameters:

- input impedance R_i<500Ω;
- power supply V_{DD}=±1.25V;
- current gain A_i equal to 1 or 5.

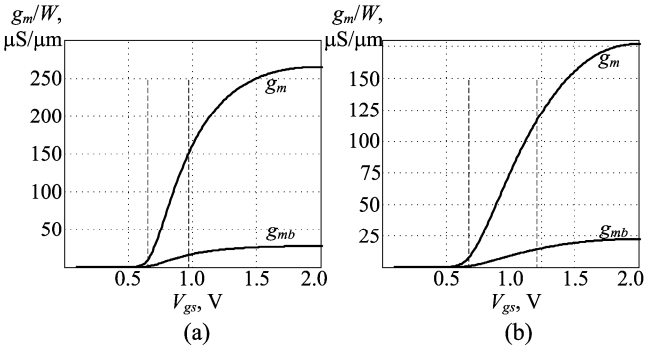

Fig. 2. Transconductances g_m and g_{mb} vs. gate-source voltage, normalized by the width: a) NMOS; b) PMOS. The drain-source voltage is 1.25 V.

The minimum gate length of the 2.5V MOSFETs in the used process is 270nm. It is good practice to use at least two times the minimum technology feature size to minimize the device mismatch. Since the process is 32nm, the minimum 2.5V transistor gate length is well over the minimum feature size. Transistors with 270nm channel length will be used to achieve maximum frequency bandwidth at the specified power supply voltage.

The specified input impedance determines the value of M_1 and M_3 transconductances. They can be estimated using formula (2), taking into account that g_m and g_{mb} for both input transistors have to be equal and using the worst case value of 10% for g_{mb}/g_m:

$$g_{m1} = g_{m2} = g_m = \frac{1}{2.2R_i}\ . \quad (5)$$

From (5) it follows that g_m must be higher than 910 µS.

The transconductances of M_1 and M_3, assuming long channel devices, are respectively:

$$g_{m1} = \sqrt{2\mu_n C_{ox}\frac{W_1}{L} I_d}\ ; g_{m2} = \sqrt{2\mu_p C_{ox}\frac{W_2}{L} I_d} \quad (6)$$

Since I_d, C_{ox} and L are equal for both transistors the transconductances of M_1 and M_3 are equal if:

$$W_1/W_2 = \mu_p/\mu_n\ . \quad (7)$$

Due to the short channel effects this expression is not quite accurate and graphical methods will be applied for obtaining proper widths of M_1 and M_3.

Drain current and transconductance vs. V_{gs} for NMOS transistor, normalized by channel width are plotted simultaneously on Fig. 3(a). The first step is to select a normalized value for g_m – it is better to be in the middle of the area, where g_m is linear function of V_{gs} (marked by dashed lines in Fig.2)[5]. The choice here is 91µS/µm and it directly gives W_1=10µm. Next step is to find V_{gs} of M_1 and its normalized drain current as it is shown in Fig. 3(a). They are V_{gs}=830mV and I_d/W=9µA/µm, which gives I_d=90µA. The normalized value for the drain current of M_1 should be in the area of the square law dependence. If it is not, different starting point should be selected.

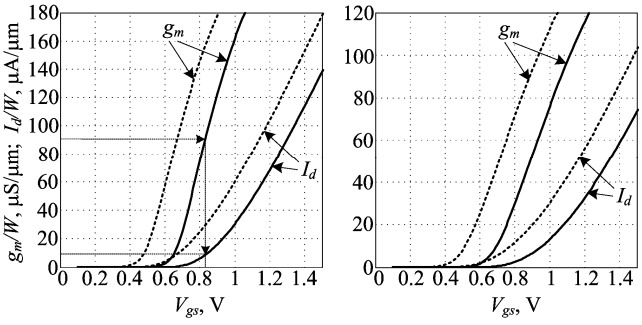

Fig. 3. Plots of normalized g_m and I_d vs. V_{gs}: (a) NMOS; (b) PMOS. Dashed curves are at V_{bs}=0, solid lines are at V_{bs}=1.25V.

The M_3 channel width has to be set to a value, which ensures the same transconductance at the same drain current as in M_1. A convenient way to do this is to plot a family of $g_m(I_d)$ curves at different channel widths (Fig. 4). The target point "a" (I_d=90µA and g_m=910µS) falls between W=24µm and W=25µm and approximately corresponds to W=24.7µm. This value is used to calculate the normalized values for g_m/W=36.8µS/µm and I_d/W=3.6µA/µm of the PMOS transistor. To make sure M_3 operates in saturation these points are cross-checked in Fig. 3 (b). It should be in the region where g_m/W increases linearly and I_d/W changes quadratically.

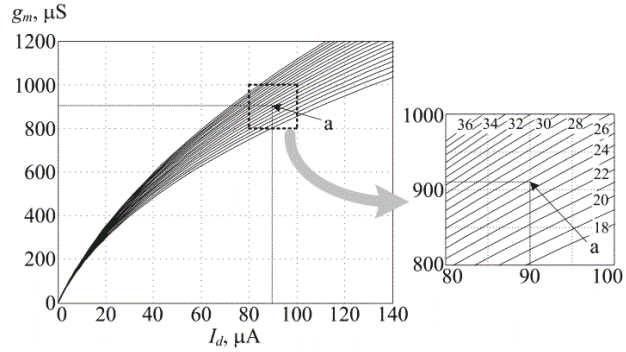

Fig. 4. Family of curves $g_m(I_d)$ for PMOS at different channel widths. In the zoomed picture the channel widths are marked on the corresponding lines.

The obtained widths provide matching of the input transistors pairs (M_1/M_3). The same sizes will be used for the other pairs (M_2/M_4, M_5/M_7, M_9/M_{11} and M_{10}/M_{12}), since they ensure the necessary current for proper operation. The output transistors M_6/M_8 are an exception since their sizes is defined by the current gain.

This is first approximation for the device sizes assuming no channel length modulation. In reality, the drain current depends on drain-source voltages, which are unknown initially. An operating point analysis returns the real picture in the circuit. It is done at I_b=90µA and the received parameters of interest are shown in the first row in Table 1. The reason for the deviation from the desired values is the large difference between real V_{ds} values (V_{ds1}=601mV, V_{ds3}=586mV) and V_{ds}=1.25V used in simulations so far.

The values of g_m and I_d through M_1 and M_3 are lower than the target values, which is consequence of the non-ideality of the current mirrors. They are compensated by increasing of the referent current to I_b=133µA applying parametric analysis and using the value of M_1 and M_3 transconductances as a criterion. The results are given in the second row of Table 1. It can be further optimized by a new parametric analysis, taking as a parameter the ratio between the widths of PMOS and NMOS transistors, and using as a target the difference between g_{m1} and g_{m3}. The third row of Table 1 shows that the matching is very good at widths W_1=10µm and W_3=23.7µm.

The widths of M_6/M_8 should be 5 times larger when A_i=5 (W_6=50µm and W_8=118.5µm) and the same as the other transistors widths at A_i=1.

TABLE 1: CHANGE OF THE BASIC PARAMETERS OF M1-M4 DURING THE DESIGN ITERATIONS

Itera-tion	I_{d1}, µA	g_{m1}, µS	I_{d3}, µA	g_{m3}, µS	I_{d2}, µA	g_{m2}, µS	I_{d4}, µA	g_{m4}, µS
I	67.6	758	67.6	750	80.3	849	77.5	823
II	95.8	911	95.8	927	116	1032	112	1028
III	95.5	909.5	95.5	910.5	116	1032	111	1010

IV. EVALUATION OF THE DESIGNED AMPLIFIER

After final device sizing and confirming that the desired operating point is achieved, it is necessary to check and investigate the other circuit parameters. The frequency dependent parameters of the amplifier – current gain and the magnitude of the input impedance at different load resistances – are considered first and their plots are given in Fig. 5. The current gain at short circuited output (R_L=1Ω and R_L=10Ω) is about 10% higher than the desired value. If an exact gain of 1 is required, the widths of the output transistors (W_6 and W_8) should be modified accordingly. The current gain decreases as the load resistance becomes comparable to the output impedance of the amplifier. The output impedance can be calculated by (3), where g_{ds6} and g_{ds8} are directly obtained from the simulation and it is 12.4kΩ. The corner frequency at -3dB decreases as R_L increases: ~2.3GHz at 1Ω, 10Ω, 100Ω; 1.82GHz at 1kΩ; and 664MHz at 10kΩ. This dependence is basically due to the increased output voltage when R_L is high, which increases the Miller effect of the drain-gate capacitance of M_6 and M_8.

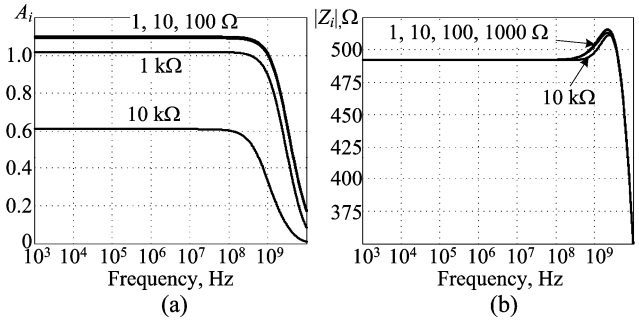

Fig. 5. Frequency responses of (a) the gain and (b) the input impedance of the amplifier, designed for A_i=1, at different loads.

The input impedance shown on Fig. 5(b) practically is constant up to 1GHz. Its value is 492Ω - very close to the specified upper limit for this parameter. This limit was used as a target parameter in the design – thus, there is a very good convergence between the target and the simulated input impedance. However, a good practice is to provide some margin for the target in order to compensate possible deviations due to process variations, temperature etc.

The amplifier, designed for A_i=5 has similar behavior. Its simulated low frequency gain is a bit higher than specified – 5.46, and the input impedance does not change. Due to the bigger output transistors and higher currents through them, the corner frequency is lower and vary from 1.04GHz at R_L=1Ω to 175MHz at R_L=10kΩ. Output impedance is also lower – 2.52kΩ.

The linearity of current amplifiers is usually demonstrated by DC transfer characteristic (output vs. input current). The plot is impressive, however it does not describe well the non-linearity as it is very close to straight line and a numerical criterion is missing. Also, there is no information on how non-linearity is affected by the frequency. These weaknesses are avoided here and in Fig. 6 are shown the dependence of the amplitude of the output current and its total harmonic distortion (THD) from the amplitude of the input current. This is done at two different frequencies – 1kHz and 300MHz, and at two different loads - 1Ω and 1kΩ. Obviously, nonlinear distortion represented by THD increase at high frequency, but this can be seen only on the plot of THD in Fig. 6(b).

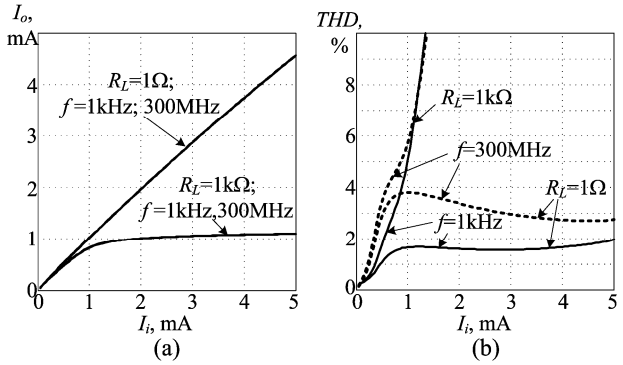

Fig. 6 (a) Dependence between amplitudes of the output and input currents at two different loads and two different frequencies; (b) THD of the output current vs. the amplitude of the input current.

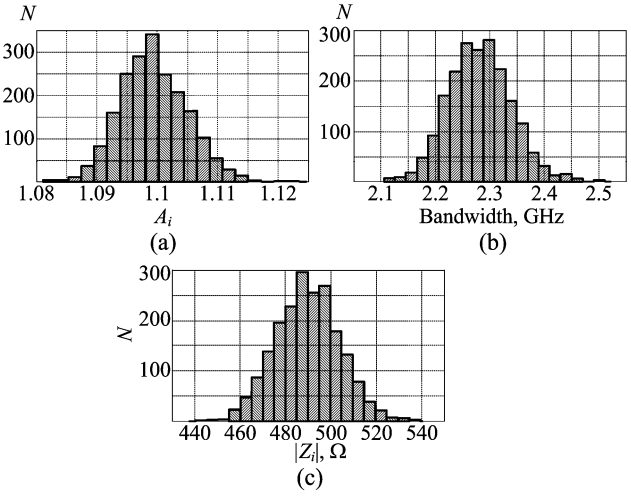

Fig. 7. Monte Carlo analysis of the circuit (2000 runs): (a) current gain; (b) frequency bandwidth at -3dB; (c) input impedance.

The last investigation is about the influence of the process variations. It uses the information about statistical variations during chip manufacturing, included in the IBM process design kit for this technology [10]. The histograms on Fig. 7 demonstrate the deviation of the three major parameters: current gain, bandwidth determined at -3dB and input impedance. The main conclusion is that they are reasonably stable and the variations are within ±10% for the bandwidth and input impedance and ±3% for the current gain.

V. CONCLUSION

The considerations concerning the design of a current amplifier, done in the paper, are focused mainly on several targets: ensuring of the desired gain and input impedance of the amplifier, and achieving good symmetry between upper and lower halves of the amplifier. While the first two are small signal parameters, the last one (symmetry) determines the linearity of the circuit. The difficulties in the design are caused by the different types of transistors, used in the upper and bottom parts of the circuit, and by the typical problems existing in the modern short channel technologies. The procedure, proposed here to overcome these problems, combines the basic theoretical formulas, graphical methods and computer simulation. Its target is proper sizing of the transistors at optimal operating point.

The considerations are illustrated by design of a current amplifier. This example demonstrates the good matching between the specified parameters and those, obtained by computer simulation of the designed amplifier. The sensitivity concerning the process variation is investigated by Monte Carlo analysis. It is small, since the used process (IBM CMOS32LP) is well established, but also due to the good design centering, achieved by the proposed procedure.

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