Modelling, Simulations and Design Considerations for Inrush Current Limiting Topologies

Radko Stoyanov Stoyanov, Emil Ganchev Rosenov, Angel Stanimirov Marinov and Vencislav Cekov Valchev

Abstract – **The current paper is focused on analyzing various inrush current limiting techniques used in a wide range of single phase AC applications. Directions for selecting the best topology for a particular design are presented, based on modeling and simulations in MATLAB. The simulation models allow the user easily to determine the correct solution for a given application in terms of losses (during the limiting process and in steady state operation), current and voltage rise by di/dt and dv/dt.**

Keywords – **Inrush current limiting, start-up circuit, MATLAB modeling, lowering the steady state losses, grid voltage dips.**

I. INTRODUCTION

With the exponential growth of the technologies using Switched-Mode Power Supplies (SMPS) there is a constant need of choosing the proper inrush current limiting technique in a particular application. Because of the large capacitors used in the SMPS a large inrush currents flow during the start-up of a device. This is true even in the low power SMPS applications like the 90 W laptop adapter presented in [1]. The current paper presents a possible solution of determining the most proper technique when inrush current limiting is required. There are few known solutions widely used in the practice and each has its positive and negative aspects, which makes it very difficult to choose the right one. The proposed MATLAB model shows the most common circuit when a SMPS is employed. It consists of an input filter, rectifier and three typical blocks of current limiting, see fig. 1. The first one utilize a resistor with the proper power, which is used to limit the initial currents when a SMPS is switched-on, and when the steady state operation of the scheme is established the resistor is commuted by a relay. The second approach uses a Negative Temperature Coefficient (NTC) thermistor that has high initial resistance during start-up, which drops to some few tenths of an ohm when heated up. The last solution reviewed by this paper employs a MOSFET's turn-on characteristics used to limit the inrush currents. The model gives a graphical representation of the main parameter used when a start-up circuit is designed (losses during the limiting process and losses in steady state operation, current and voltage rise by di/dt and dv/dt) which helps the user to easily determine the correct technique.

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II. MAIN PARAMETERS AND TECHNIQUES IN INRUSH CURRENT LIMITING CIRCUITS

The internal losses in a SMPS are caused primarily in the following factors [2]:

Magnetic component losses - "skin effect" and "proximity effect";
Power switch losses - saturation losses and switching losses;
Quiescent power losses - start-up supplies, inrush current limiters.

The latter is discussed in details in this paper. Inrush current limiting circuit should protect the consecutive components. To do so it needs to be well designed.

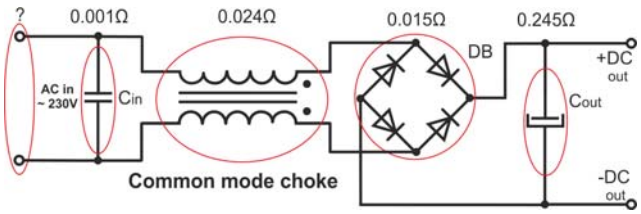


Fig. 1. Input part of a SMPS – most common design. The figure represents the main components of a standard SMPS: input filter, rectifier bridge and output filter.

A. Inrush currents when no limiting is employed

If no measures are taken to limit the inrush current, they are limited only by the parasitic impedance of the components presented in fig. 1 and in [3]. It results in the following numerical equations:

$$V_P = 230.000 \times 1.100 \times 1.414 = 357.742V \quad (1)$$

V_P – *peak input voltage*

$$R_S = R_{ci}+R_f+R_r+R_{co} =$$

$$= 0.001\Omega + 0.024\Omega + 0.015\Omega + 0.245\Omega = 0.285\Omega \quad (2)$$

R_S – *series resistance*

$$I_{inrush} = \frac{357.742V}{0.285\Omega} = 1255.235A \quad (3)$$

I_{inrush} – *peak inrush current*

As it can be seen, the parasitic elements alone are not sufficient to limit the inrush currents. To do so additional impedance should be added to the series resistance of the circuit. There are few known topologies typically used for that purpose. A summary of these circuits is presented in fig. 2.

B. Inrush current limiting topologies

Each of the shown circuits offers advantages and disadvantages to the SMPS design and some are discussed below:

- The circuit shown in fig 2 a) is the easiest to design but with NTC the inrush currents are still large and there are much losses in high power applications
- The second one (fig. 2b) serves the larges variety of applications but there are also much losses during start-up and a second peak in the current when the relay shortens the ballast resistor. It is also the least reliable one since there could be pitted contacts on the relay.
- The circuit shown in fig. 2 c) is decent in low power applications. It offers a steady charge of the output capacitor but there are constant loses in the switch during operation and the ground wire is disturbed by the switching process. Some possible solutions of eliminating the latter problem are discussed in [4], [5].

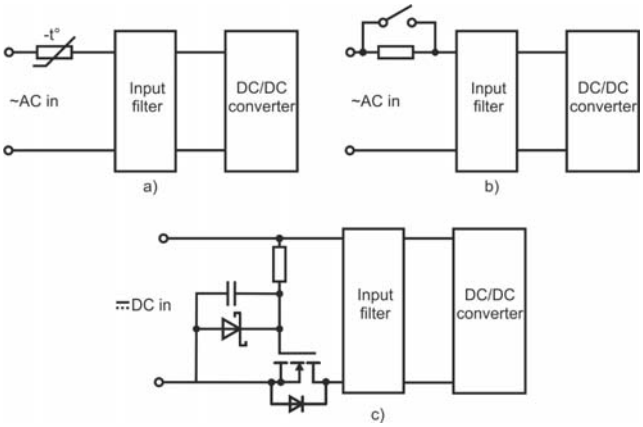


Fig. 2. Power supply inrush current limiting techniques: (a) NTC thermistor technique; (b) resistor-relay technique; (c) MOSFET-based approach [40].

III. MATLAB MODELS AND MEASUREMENTS

Three MATLAB models are presented in this paper covering the topologies discussed in the previous chapter. There are many simulation software products on the market today and it is rather difficult to choose in between. This article is based on MATLAB Simulink models because they offer larger complexity and flexibility compared to PSpice Capture let's say, where it is easy to represent a particular solution with ready to use library components.

The first model presented in fig. 3 a) uses a heat source controlled by a signal representing the recommended from the manufacturer law to operate the different NTCs required for different power applications.

The second model uses a variety of high power resistors to limit the inrush currents until the output capacitor is sufficiently charged, then a voltage feedback senses a selected threshold and triggers the relay, which on its hand shortens the ballast resistor see fig. 3b).

The last model represents the MOSFET based inrush current limiting topology, where a power MOSFET is controlled by a passive circuit that offers a slow turn-on of the switch (means slow decrease of the ON resistance to its nominal value of few tenth of an ohm) resulting in the smooth charge of the output capacitor. This circuit is presented in fig. 3 c).

A. Inrush current measurements

In this part, the MATLAB models and the received results are discussed. First a graphical representation of the inrush currents in the three models is given. To generalize the complexity of the three circuits, they are compared in a wide power range. In the first circuit four NTC thermistors are used with a proper values recommended by the manufacturer for 1 A, 5 A, 10 A and 15 A load current to give the users a proper impression of what inrush currents one can expect to a corresponding power [6].

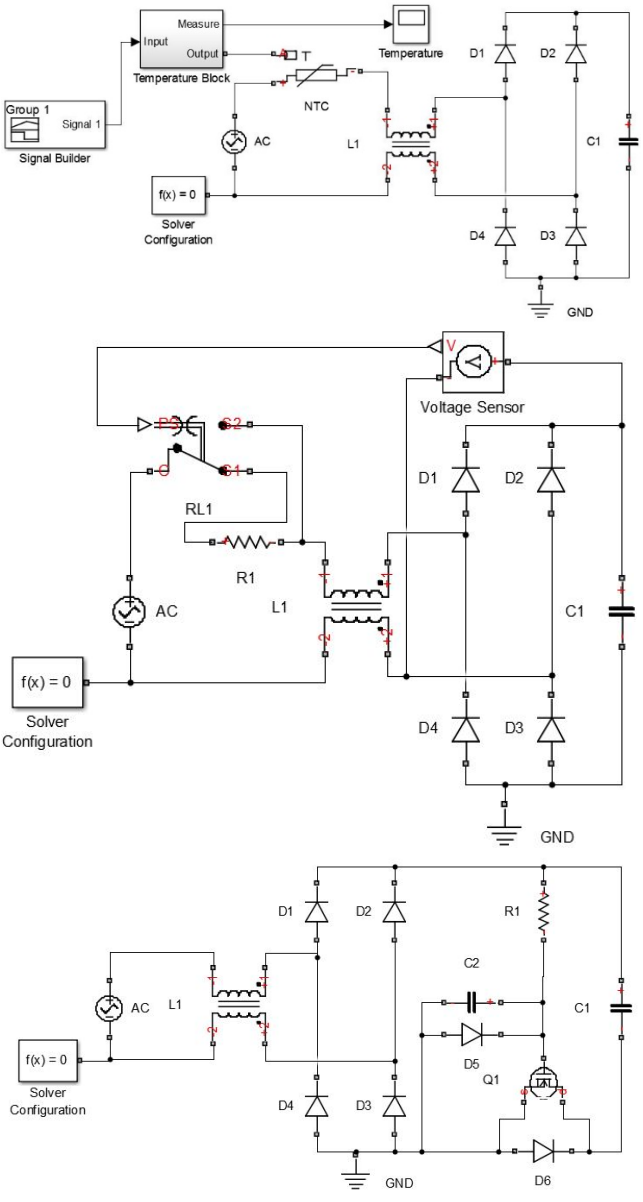


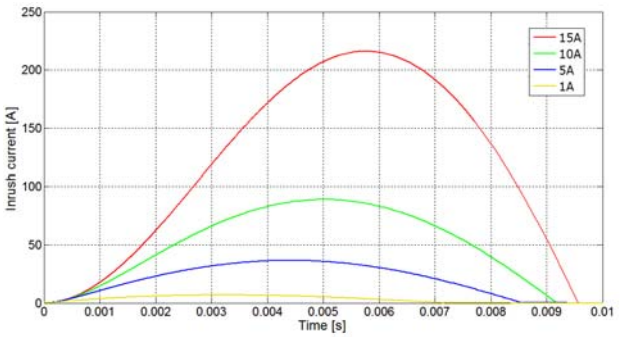
Fig. 3. MATLAB models used to compare the three topologies: (a) NTC thermistor based technique; (b) resistor-relay technique; (c) MOSFET-based technique.

The results of the conducted simulations of the NTC based topology are summarized in fig. 4a, as can be seen the inrush currents with this topology are still sufficient. They are in the range few amperes to more than 200 A.

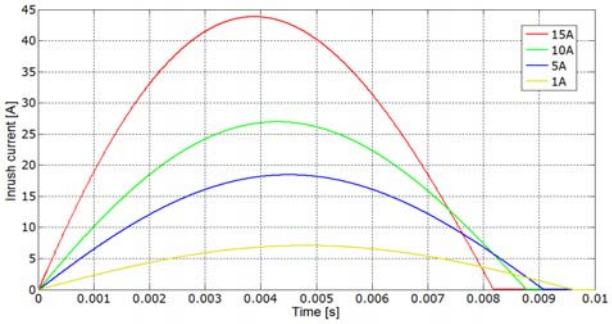
The relay approach offers larger limiting abilities compared to the previously discussed method because of the variety of ballast resistors possible. The inrush current in this case is largely reduced and varies from few amperes to less than 45 A. Both methods use non-controlled impedance to limit the inrush current so the largest value is in the first half-period of the sine wave.

In addition, many components that can be damaged (rectifier diodes) by the inrush currents have its value for 8.3 ms listed in their datasheets. The values of the proposed by the author NTCs and ballast resistors is summarized in a table below.

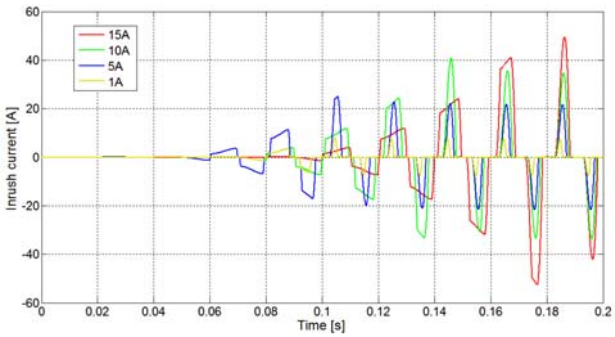
The third method uses a passive control circuit to operate the inrush current limiting MOSFET, which means that the inrush current can be managed as required. In the graph presented in fig. 4 c) there are several periods of the limiting cycle so it is clear how smooth the capacitor can be charged via this method. It is important to note that the last topology is tricky to design and operate compared to the previous ones.



a)



b)



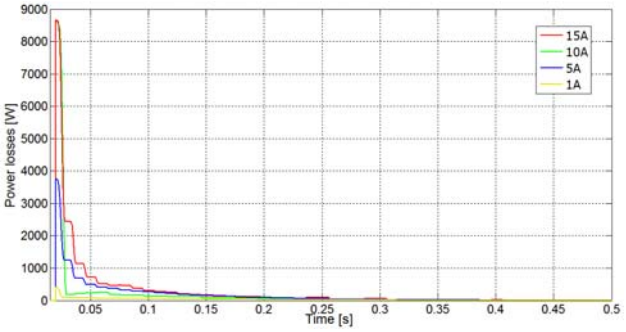
c)

Fig. 4. Inrush currents in the three basic topologies: (a) NTC thermistor based technique; (b) resistor-relay technique; (c) MOSFET-based technique.

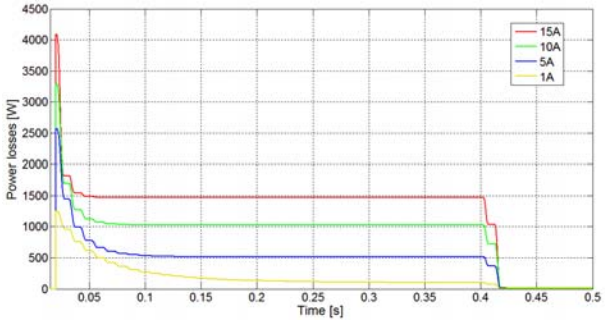
B. Power losses measurements

When designing an inrush current limiting circuit there are several parameters to be considered. The first one is the amplitude of the inrush current, then there are power losses and price of the solution and each one can be divided in subsections. The power losses for example can be losses during the start-up process and steady state losses. The transient losses (during start-up) are caused by the large initial value of the limiting impedance while the steady state losses are caused by the constant impedance left in the circuit after the transient process. For a better understanding, those losses are further explained and shown in separate diagrams and then summarized in a table.

The graph shown in fig. 5 a) presents the transient power losses at the NTC based circuit. It can be seen that the major part of these loses is concentrated as a high spike in the beginning of the cycle. This is because of the low initial resistance of the NTCs compared to the other current limiting components. In fact, the steady state resistance of the NTC can drop with some 50 to 100 times compared to the initial value.



a)



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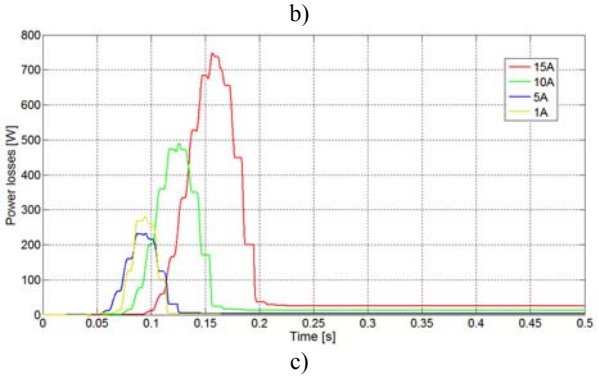

c)

Fig. 5. Transient power losses in the three basic topologies: (a) NTC thermistor based technique; (b) resistor-relay technique; (c) MOSFET-based technique

The transient losses in the second circuit are much higher because of the large impedance of the ballast

resistors, see fig. 5 b). This is the reason why the resistance needs to be commutated out after the initial charge of the capacitor.

Because of the dynamic control, the transient losses in the last circuit are the lowest according to fig. 5 c). Even so, the MOSFET needs to be protected against high voltage spikes.

After the initial charge of the output capacitor (often 0.5 s up to 1 s) the inrush current limiting circuits are in steady state operation until the next power-on of the device. During that time the second type of losses (steady state) occur. In the case of the circuit presented in fig. 3 b), this is the standby power consumed by the relay - typically 1÷2 W. In the MOSFET circuit there are constant loses due to the on state resistance presented in fig. 6.

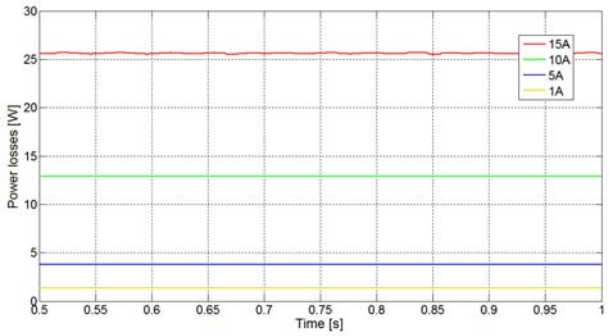

Fig. 6. Steady state losses in a MOSFET-based topology.

It can be seen that in high power the losses in the switch become are significant. This is the second reason why the MOSFET topology should be used for low power applications.

The NTC resistance when heated up is also relatively linear. The steady state losses of the three methods are compared in table 1.

TABLE 1. STEADY STATE LOSSES

	NTC	Relay	MOSFET
1 A	0.6 W	1-2 W	1 W
5 A	2.9 W	1-2 W	4 W
10 A	4.7 W	1-2 W	13 W
15 A	5.9 W	1-2 W	26 W

For the power range discussed in this paper, NTC's with the following initial and steady state resistances are proposed in the table 2.

TABLE 2. INITIAL AND STEADY STATE RESISTANCE

	NTC In	NTC St	Relay In
1 A	10 Ω	0.340 Ω	47 Ω
5 A	2.5 Ω	0.044 Ω	16 Ω
10 A	1 Ω	0.018 Ω	10 Ω
15 A	0.5 Ω	0.01 Ω	5 Ω

The steady state resistances for the relay base circuit is determined by the contact resistance, which is negligibly low.

Table 1 shows that there is a preferred solution for each power range. It is recommended to use MOSFET based circuit for low power applications because of the significant losses if there are high currents presented. The relay circuit is preferred in high power applications because of the relatively low losses compared to the other two circuits. The NTC circuit is advisable to be used in between because of its simplicity an relatively low price. The drawn conclusions are summarized in fig. 7.

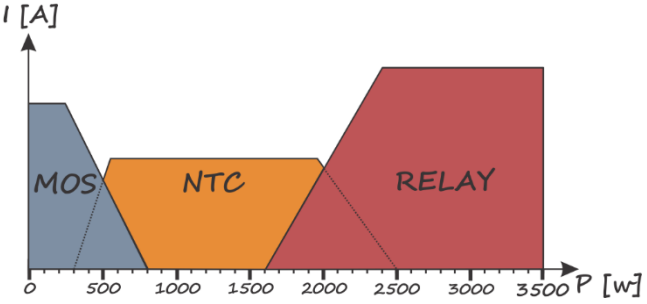

Fig. 7. Proposed range of inrush current limiter techniques based on the studied current amplitudes and application power.

V. CONCLUSION

The main parameters while limiting the inrush currents are summarized. A MATLAB model for selecting the design parameters in a particular design is proposed. It allows the user to model inrush current limiting topologies. Directions for selecting the best topology for a particular design are presented. The simulation models allow the user easily to determine the correct solution for a given application in terms of losses (during the limiting process and in steady state operation), current and voltage rise by di/dt and dv/dt.

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