Unified Method for Behavioral Modeling of IGBT

Tsvetana Grigorova Grigorova and Katya Konstantinova Asparuhova

Abstract – **This paper presents a complete behavioral PSpice model for IGBT transistor. A voltage dependent capacitance is modeled using a second order polynomial and "arctan" function.**

The simulation results for I-V static and transfer characteristics and their comparisons with datasheets are shown. The dynamic model verification is carried out using PSpice simulations and experimental measurements of the circuits with active and inductive clamped loads.

Keywords – **IGBT Behavioral Model, Nonlinear Capacitor Modeling**

I. INTRODUCTION

The IGBT was introduced into the family of power devices to overcome the high on-state loss while maintaining the simple gate drive requirements of power MOSFETs. The IGBT combines both bipolar and MOSFET structures and possesses the best features of both devices types. Because the IGBT has a low power gate drive requirement, a high current density capability and a high switching speed it is preferable to other devices in many power applications and a practical circuit model for IGBT is needed for simulation. Several analytical models have been implemented into circuit simulators (PSpice and Saber) in recent years. The IGBT models available in literature can be subdivided as either behavioral or physics-based. The physics-based IGBT models proposed to date, are not easily implemented in circuit simulators, require heavy numerical computations and the knowledge of process parameters, which are not easy to extract from electrical measurements. A significant part of existing behavioral macromodels [1,2,3] are physical, based on the internal device structure. The others, considering the semi-empirical relations between terminal voltages and currents, have a poor accuracy and their results are valid only in a narrow range of operating conditions.

However the model still presents some limitations in the saturation region at where the collector current is assumed flat. Real IGBTs show that the collector current slightly increases with the collector-emitter and gate-emitter voltages. In this paper, an improvement to the model is given to overcome this limitation.

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II. MODEL DESCRIPTION

A. IGBT DC Model

The DC part of the proposed model is based on the empirical formulas (1) for the IGBT collector current given in [5]. This part combines the equations that describe the MOSFET in cutoff, the linear and saturation regions with the equations of a bipolar junction transistor operating in the active mode. The model accounts for high-level injection and the voltage drop in the extrinsic part of the IGBT. The meaning and the extraction of individual factors and functions are described in details in the same paper.

$$I_C = \begin{cases} 0, & if \quad V_{GE} \le V_{th} \quad or \quad V_{CE} < V_D \\ k.f_2 \begin{bmatrix} (V_{GE}-V_{th})(f_1 V_{CE} - V_D) - \\ -\dfrac{(f_1 V_{CE} - V_D)^2}{2} \end{bmatrix} \\ if \quad V_{CE} < V_{GE} + V_D - V_{th} \\ k.f_2 \dfrac{(V_{GE}-V_{th})^2}{2} - K(V_{GE}) \cdot (V_{CE} - V_{th}), \\ if \quad V_{CE} > V_{GE} + V_D - V_{th} \end{cases} , \quad (1)$$

where $K(V_{GE})$ represents the slope at a given gate – emitter voltage

$$K(V_{GE}) = \frac{I_{sat}(V_{GE})}{V_{early} + V_{th}}, \quad (2)$$

where V*early* is similar to the Early voltage in the BJT.

B. Dynamic model of IGBT

The dynamic model is presented on Fig. 1. The transient waveforms are modeled with good accuracy using the three capacitors C_{CG}, C_{GE} and C_{CE}. The values of the capacitors can be extracted from the dependence capacitance vs. V_{CE} for $V_{GE}=0$.

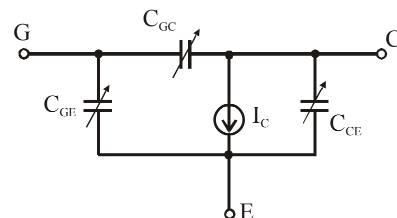


Fig.1. Dynamic behavioral model

From the datasheets, three capacitance curves can be obtained for extraction of C_{CG} and C_{GE}:
$C_{ies} = C_{GE} + C_{GC}$, $C_{res} = C_{GC}$, $C_{oes} \approx C_{CE} + C_{GC}$, where C_{ies} is the input capacitance, C_{res} the reverse transfer capacitance, and C_{oes} the output capacitance. To achieve an accurate description of IGBT's switching waveforms, it is necessary to develop a high precision model for C_{GE}, C_{GC} that exhibit nonlinear variation of the corresponding voltages.

In the previous work [4] a voltage dependent capacitance can be specified by using a look-up table. This voltage dependent capacitance is the multiplied by the time derivative of the voltage to obtain the output current. For the better convergence of the iterations process and avoiding problems we recommend the two different approaches.

First, the reverse transfer capacitance $C_{res} = C_{GC}$ can be modeled with a polynomial. For example, Fig.2 shows the digitizing values from data sheets of the voltage depend capacitor and its modeling with second order polynomial. The polynomial coefficients are calculated using Mathcad program.

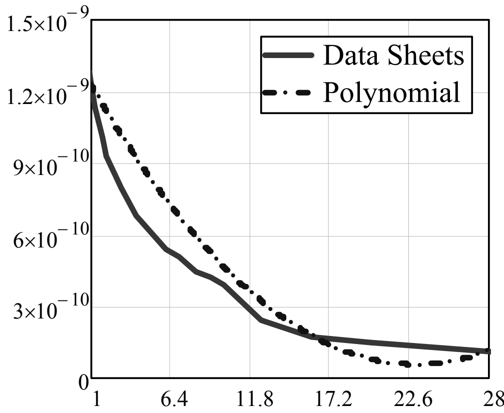


Fig. 2. Comparison of digitizing values of the reverse transfer capacitance from data sheets of the voltage dependent capacitor and its modeling with second order polynomial

The second approach for a modeling the IGBT voltage depend capacitor includes using a function "*ATAN*" because of its smoothness (Fig.3) [6].

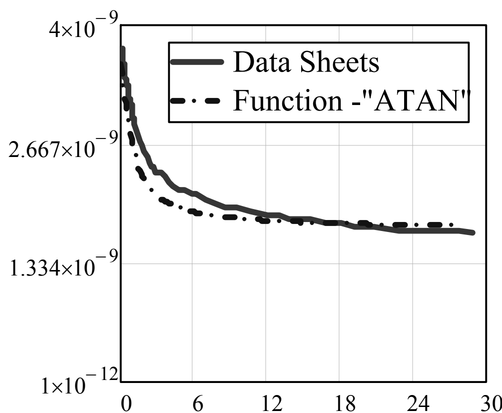


Fig. 3. Comparison of digitizing values of the input capacitance from data sheets and its modeling with a function "*ATAN*"

The process of the device switch over is modeled using a voltage-controlled switch S with parameters: $V_{on} = \{V_{th}\}, V_{off} < \{V_{th}\}, R_{on} = \{V_{CE(sat)}/I_C\}$ and R_{off} - a very big value corresponding on turn-off transistor.

III. IGBT PSPICE Model Implementation

The behavioral model described above has been developed using ABM method and implemented in the OrCad PSpice simulator as a subcircuit. The DC part of the IGBT model includes the voltage control current sources GVALUE which implement Eqs. (1), using "IF-THEN-ELSE" operator in PSpice. The correction functions f_1 and f_2 realize using GPOLY source [4].

Fig. 4 shows a subcircuit in which a nonlinear capacitor is modeled. The capacitor is replaced by a controlled current source, Gpoly_cap, whose current is defined by

$$I = C(V)\, dV/dt \tag{3}$$

In the subcircuit, the time derivative, dV(t)/dt, is measured by applying a copy of the voltage across Gpoly_cap to a known capacitance, Cref, and monitoring its current. The *C(V)* function in the subcircuit is arbitrary [7]. The value of the nonlinear capacitor model in this example has a second order polynomial dependence on its voltage. The graphs *C(V)* from datasheet are digitizing using an appropriate program like GetData.

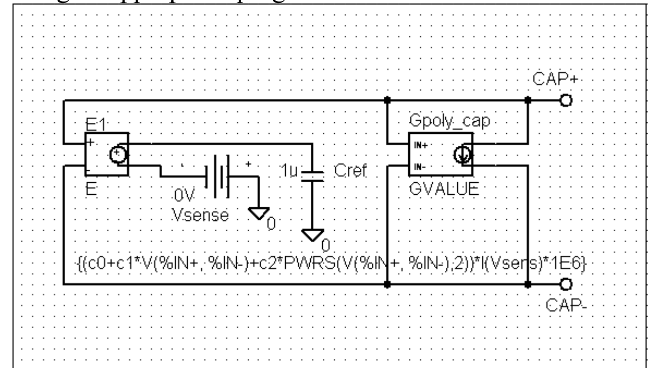


Fig.4. Nonlinear Capacitor with Polynomial Expression

The realization in Spice language a function "*ATAN*" is with GVALUE voltage control current source:

$$value = \{(d0 + d1 * ATAN(V(\%IN+,\%IN-)) * DDT(V(\%IN+,\%IN-))\} \tag{4}$$

An advantage of the proposed model that it is parameterized. It allows easy implementations of the different IGBT types. A part of the preliminarily extracted parameters are included in Param operator – these are V_{th}, V_D, β, k_p, the coefficients a_0, a_1, a_2; b_0, b_1, b_2 of the correction functions f_1 and f_2. The parameters of the voltage-controlled switch are parameterized too.

IV. Simulation and Experimental Results

For the verification of the model the type FGA90N33AT IGBT [8] is chosen. First, the DC part of

the model is compared with the corresponding characteristics from the data sheet.

A. Simulation Results

In the calculation it was assumed that V_{th}=4V, β=100, k_p=1.01. The values of the correction functions coefficients in this model realization are:

a_0 = -0.12 a_1 = 1.483 a_2 = -3.11 for f_1

b_0 = -0.00462 b_1 = 0.09 b_2 = -0.462 for f_2.

The simulations are made under following initiation conditions: V_{CE} = 0÷6V, V_{GE} = 6÷8V. Fig. 5 shows the static I-V characteristics offered by the behavioral macromodel .

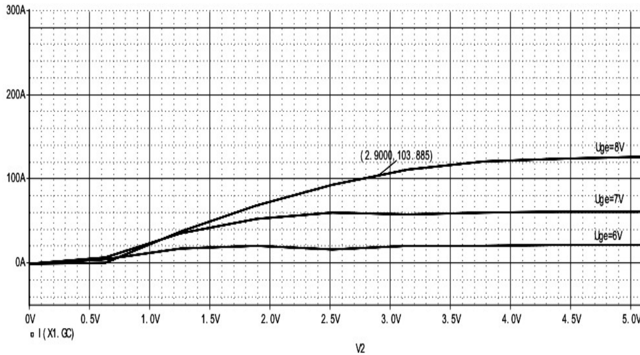


Fig.5. Behavioral macromodel simulated static I-V characteristics for the device FGA90N33AT

The analyses results are summarized and compared in Table 1.

TABLE 1. I-V CHARACTERISTICS COMPARISON

U_{GE},V	Data Sheet		Behavioral macromodel		Error, %
	U_{Csat},V	I_{Csat}, A	U_{Csat},V	I_{Csat}, A	
8	2.98	103.584	2.9	103.885	0.2
7	2.2513	54.567	2.26	57.124	4.6
6	1.25	13.873	1.25	15.65	12.7

The average error between the theoretical predictions of the behavioral model and the manufacturer's data is less 5%. The largest error occurs around V_{GE} = 6V.

Fig.6 shows the transfer characteristics received from the simulation of the proposed macromodel. The conditions are: V_{CE} = 20V, V_{GE} = 0÷10V.

The results are summarized in Table 2.

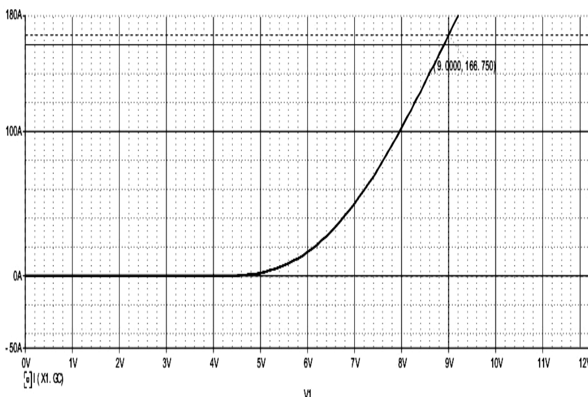
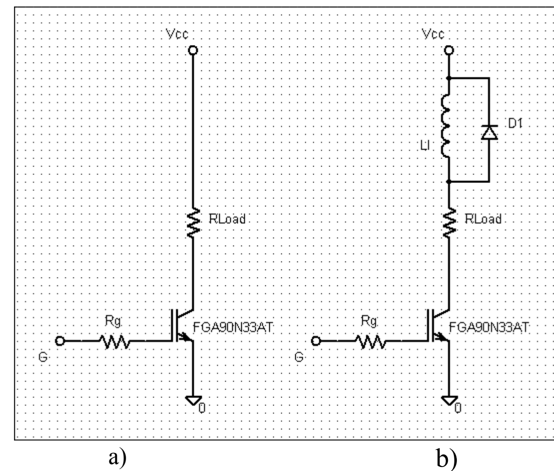


Fig. 6. Transfer characteristics characteristic for the device FGA90N33AT

TABLE 2. TRANSFER CHARACTERISTICS COMPARISON

U_{GE},V	I_C, A		Error, %
	Data Sheet	Behavioral macromodel	
7	60	54	10
8	110	102	7.2
9	160	166.75	4.2

Fig. 7 shows two transient test circuits at active and inductor load to verify the transient predictions of the proposed model.



a) b)

Fig. 7 a).Active load test circuit and b). Inductive clamped load test circuit

Fig. 8 shows the simulation results for the voltage V_{CE}, the collector current and the shape of the input impulse at the gate. The switching times: the turn-on delay time $t_{d(on)}$ and rise time t_r are recorded using the transient response, under the resistive load according to manufacturer's conditions. The conditions are:

V_{CC} = 200V, V_{GE} = 15V, $I_C = 20A$, $R_g = 5\Omega$.

The comparison between simulation and data sheets results is shown in Table 3.

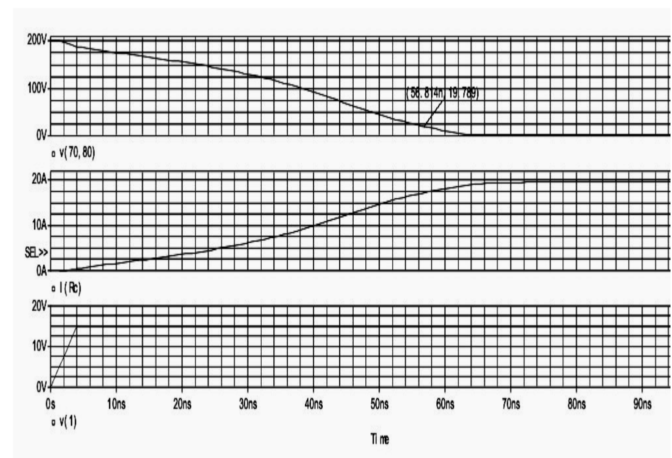


Fig. 8. Simulation results of the turn-on delay time $t_{d(on)}$ and rise time t_r

TABLE 3. SWITCHING TIMES

Parameters	Data Sheet	PSpice (Behavioral macromodel)	Error, %
$t_{d(on)}$,ns	23	20	15
t_r ,ns	40	43	7
$t_{d(off)}$, ns	100	103	2.9
t_f , ns	180	200	10

The average error between the simulation results of the behavioral model and the manufacturer's data is less than of 15%.

B. Experimental Results

The comparison between simulation and experimental results for the test circuits (Fig.7) is given in this section. The IGBT transistor is FGA90N33AT type. The conditions are: V_{CC} = 25V, V_{GE} = 12V, R_{load} =15Ω, $R_g = 5\Omega$, L_{load}=6μH, D1- MBR10100 .

Fig. 9 shows the turn-off simulation results of the collector-emitter voltage V_{CE}, load voltage V_{Rload} and gate-emitter voltage V_{GE} with active load. Fig. 10 presents corresponding experimental results.

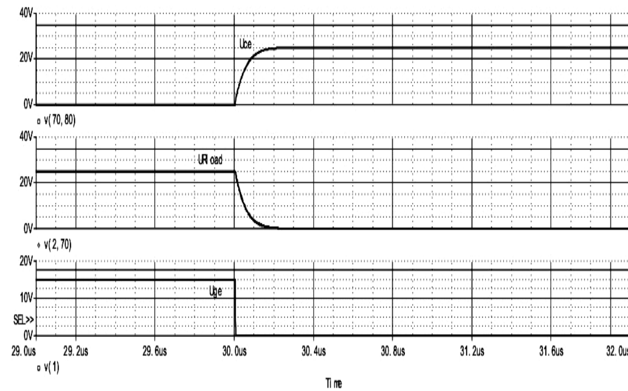


Fig. 9. Collector-emitter voltage V_{CE} , load voltage V_{Rload} and gate-emitter voltage V_{GE} .

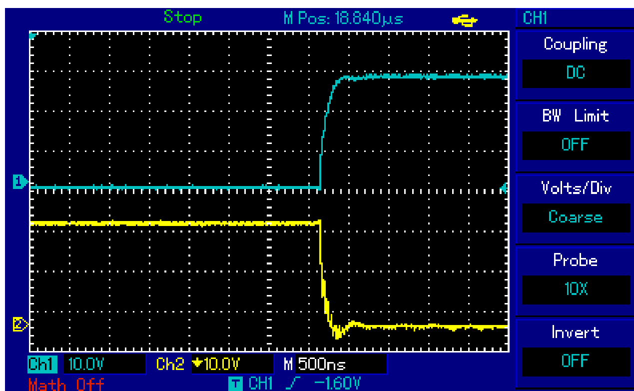


Fig. 10. Collector-emitter voltage V_{CE} and load voltage V_{Rload}

Fig.11 shows experimental results of the collector-emitter voltage V_{CE} and gate-emitter voltage V_{GE} for the inductive clamped load test circuit.

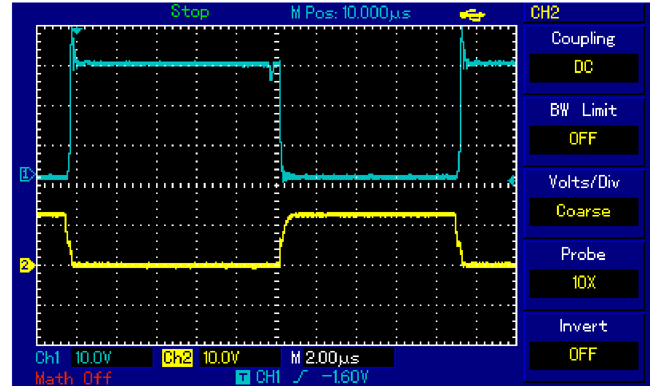


Fig.11. Collector-emitter voltage V_{CE} and gate-emitter voltage V_{GE} from the inductive clamped load test circuit

V. CONCLUSION

A complete behavioral PSpice model for IGBT transistor is presented. The using type of the IGBT is FGA90N33AT. A voltage dependent capacitance is modeled using a second order polynomial and "arctan" function.

The simulation results for I-V static and transfer characteristics are shown. The average error between the theoretical predictions of the behavioral model and the manufacturer's data is less 5%. The largest error occurs around V_{GE} = 6V.

The dynamic model verification is carried out using PSpice simulations and experimental measurements of the circuits with active and inductive clamped loads. The comparison between the manufacturer's data, the simulation and experimental results shows sufficient accuracy for the engineering calculations.

REFERENCES

[1] F. Mihalich et al., *IGBT SPICE model*, IEEE Transactions on Industrial Electronics, vol.42, No1, pp. 98-105, Feb.1995.

[2] H. S. Oh, M. El Nokali, *A new IGBT behavioral model*, Solid-State Electron., vol. 45, pp. 2069–2075, Nov. 2001.

[3] W. Kang et al., *A Parameter Extraction Algorithm for an IGBT Behavioral Mode*, IEEE Transactions on Power Electronics, vol. 19, No6, Nov. 2004.

[4] K. Asparuhova., T. Grigorova, *IGBT High Accuracy Behavioral Macromodel*, 26th Int. Conference on Microelectronics, MIEL 2008, Nis, Serbia, May 2008, vol.1, pp 185-188, ISBN 987-1-4244-1881-7.

[5] T. Grigorova, K. Asparuhova, *An Improved IGBT Behavioral PSpice Macromodel*, ICEST'2007, Bitola, vol.2, pp.785-788, Macedonia 2007.

[6] И. Недолужко. *Методика определения параметров PSpice-моделей IGBT транзисторов*, Силовая Электроника, № 2, 2005.

[7] Cadence, *A Nonlinear Capacitor Model for Use in the PSpice Environment*, App note, December 2009.

[8] http://www.fairchildsemi.com