# DC MOTOR CONTROL SYSTEMS

**Marin Hristov Hristov, Gavrail Shtilionov Kubatev, Dobromir Nikolov Arabadzhiev**

ECAD Laboratory, FETT, Technical University of Sofia, 8 Kliment Ohridski Str., 1797 Sofia, Bulgaria
e-mails: gavrail.kubatev@gmail.com, mhristov@ecad.tu-sofia.bg, dna@ecad.tu-sofia.bg

*Modern day decisions, when classifying motor controllers are divided into two categories. The first is swiftness and accuracy at the price of expensive products and the other – worse characteristics, but with more affordable prices. The presented article shows a method for digital control of a DC brush motor, and by this, showing one good decision for creating a system with good characteristics and low price.*

**Keywords:** DC motor, control system, VHDL, FPGA

## 1. INTRODUCTION

The presented control system has two main blocks – power block and a block for digital processing (fig.1). The power block is based on H-bridge scheme, level translator and an optical encoder. The mathematical processing block is physically by using a FPGA matrix. The FPGA matrix used in the project is Xilinx® XC2S100PQ208 For the implementation and development part was used Xilinx ISE Design Software made by Xilinx® and for the simulation part, the software which was used is Modelsim made by ModelTech®.The programming part was made by using language for hardware descriptions – VHDL [3,4,5].

The control part of the system is implemented in the FPGA matrix. The matrix consists of two parts – adder and a transformer.

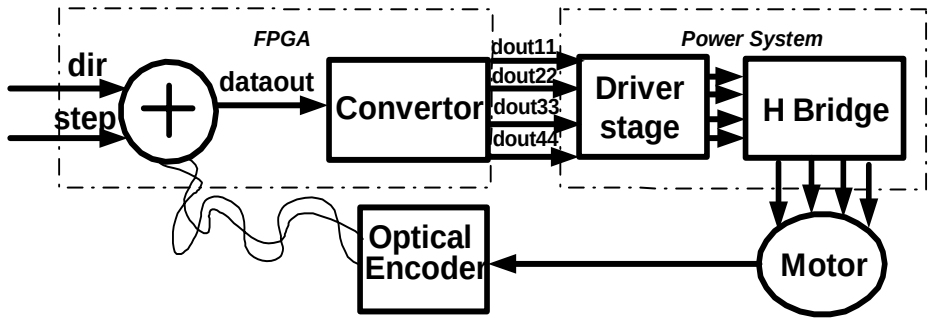


*Fig. 1 Block scheme of the system*

The input signals of the regulating system are -"step" and "dir", and the angular rotation of the motor is the output signal.

The "Step" signal is the signal which indicates the start of the motor, when it is in '1', the motor is working, when it turns to '0', the motor's movement depends only on the feedback. The "Dir" signal indicates the desired direction of movement of the motor. Those two signals are set by the user [2].

## 2.DIGITAL PART

### 2.1 Adder

The Adder is main block, which compares the assignment with the current state of the exit of the system and forms the error signal (dataout). The behavior of the adder is described by using hardware description language – VHDL.

This block has 4 input and 1output signals. Two of the input signals represent the assignment and the other two are coming from the *former*. The output signal works as an input signal for the next block – the transformer and describes its work. Block and principal scheme can be seen on fig.2.

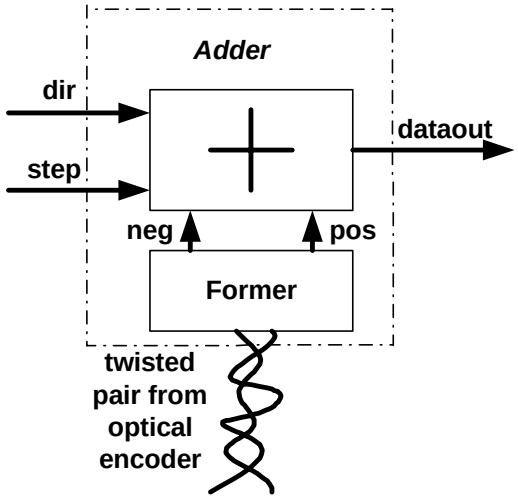


*Fig. 2.1 Block scheme of the Adder*

step - input one bit signal
dir – input one-bit signal(direction of movement)
pos- input one-bit signal ( from former)
neg – input on-bit signal ( from former)
dataout – output ten-bit signal

The processing which takes place in the adder is with the goal of transferring to the next block such a number, which describes the desired changes in the work of the motor.

The idea behind the other inner block of the adder (the former) is to transform the signals, which are coming from Optical Encoder (OE) in such a way, that they can be used by the adder. The Former has two input signals ,which are the signals coming from the OE , and two output signals 'pos' and 'neg', and if the direction of movement is clockwise ,there are impulses on the 'pos' output , and if its counterclockwise only on the 'neg' output.[2]

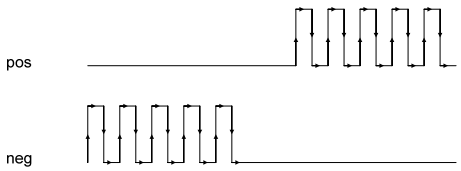


*Fig. 2.2*

The adder's way of working is based on tracking rising edges on the used signals. This is the way the output signal changes when there is a change in the state of "step" and "dir". When there is a rising edge of "step " and dir = '1', the output signal increases with 1, when there is a rising edge of "step " and "dir"= 0, the o0utput signal decreases with 1. If we look at the signals coming from the Former, if there is a rising edge of "pos", the output increases with 1, and if there is a rising edge of "neg" – decreases with one. Those two signals aren't influenced by the current state of "dir" and "step".

This simulation shows the modifying of the output signal – "dataout" depending on the current input signals. When the input signal "step" = 1 , "dir"=0, "neg" = 0 and pos ,switching between 1 and 0 , we can see at the simulation that the correct calculating of the output signal dataout , which increases. After a certain time the signal "neg" starts to switch its state and the dataout starts decreasing.

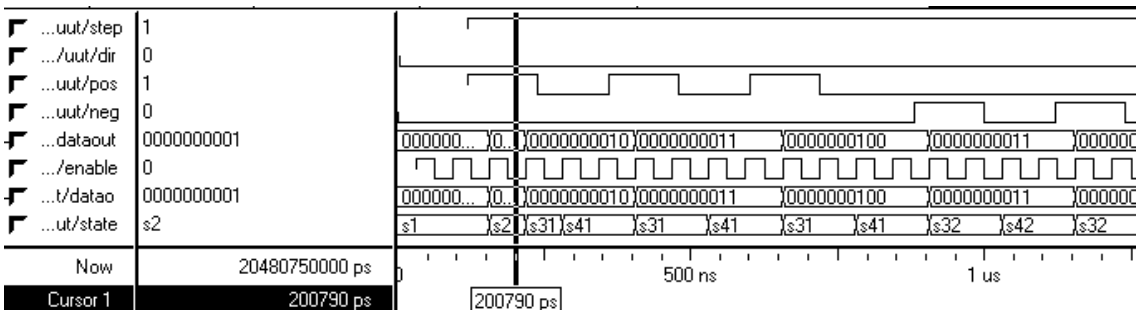


*Fig. 2.3 Simulation of the adder*

## 2.2 Transformer

The transforming block is used for ensuring the eligible duty ratio of the signals which control the H block scheme and by doing this ensuring control on the value of the suplly voltage of the motor. Block diagram of the whole transformer block can be seen on fig 2.4

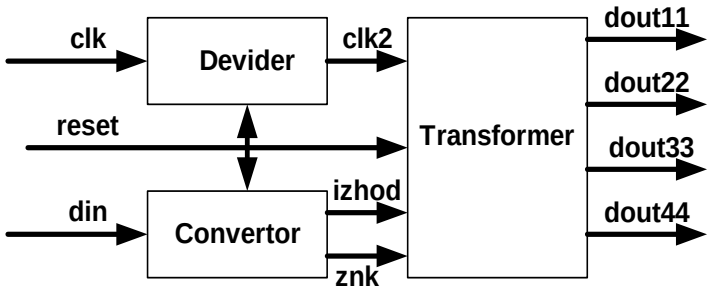


*Fig. 2.4 Block scheme of the Transformer*

din- input signal (9 bits)
clk –input frequency (32 MHz)
clk2 –divided frequency (170KHz)
izhod – signal with the processed input number (always positive)
znk –sign of the transferred by signal "izhod" number
dout11, dout22, dout33, dout44- outputs

The first component, which gets the input signal is called converter. Its purpose is to determine the sign of the incoming signal, which is in second complement and to react in a proper way. After the converter gets the number, in case it is negative, the converter must convert it into a positive one and to transfer it to the next block (with signal "izhod") for processing .If the number is positive, it is transferred without any changes. The goal of this is to make the calculations more simple and to present the data in a correct way for processing in the transformer. This component has two outputs, one of them transfers the processed number ('izhod'). And the other ('znk') its sign [2].

The second part of the block is the component divider. Its purpose is to deliver work frequency for the whole block. The input frequency of the system is 32 MHz. For correct work of the block, the needed frequency, based on the simulations and for turning off the transistors of the H-bridge scheme is 170 KHz. The component has one output, which is used to transfers impulses with frequency 170KHz.

The main component in the block is the transformer. The purpose of this component is to deliver on-bit signals to the two outputs. The outputs control the two 'shoulders/sides' of the H-bridge scheme. The signals from the converter and the divider are accepted and depending on their values the block controls the 4 one-bit

outputs. The signal coming from the divider is used as a work frequency and the signals from the converter are used for controlling the outputs. The signal for sign, controls, which one of the two pairs of outputs is active and the signals which delivers 10 bit number controls the duty ratio when switching between 1 and 0.

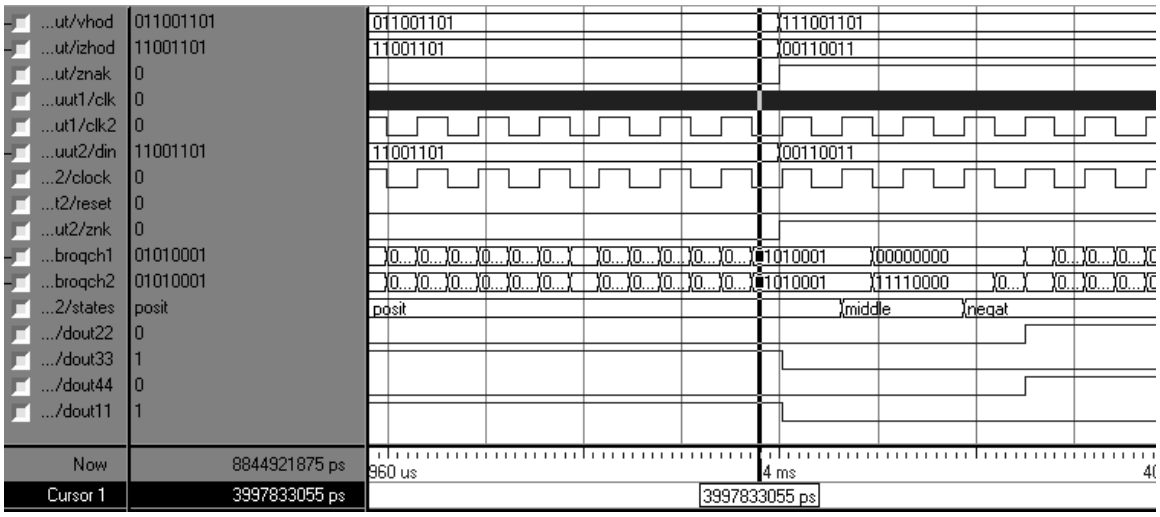


*Fig. 2.5 Simulation of the transformer*

Simulation 2 is showing, how when working with a positive input, when a negative number comes, the block reacts correctly [2] .

## 3. POWER BLOCK

### 3.1 Driver Stage

The driver stage is build of 4 bipolar transistors connected in common emitter schemes. The transistors which were used are BD 237, because of their characteristics which cover the requirement of the signals which are processed in the driver stage.

### 3.2 H- bridge scheme

The H-bridge scheme is the direct controller of the motor. When working at switch mode the 4 MOS transistors , which are controlled by the driver stage ,their duty ratio defines the work of the motor . The duty ratio vary in the range of 1 to $1/(2^9)$.

### 3.3 Feedback

The feedback is used for a detector of the motors movement, and by doing this, when there are signals transferred to the adder of the digital part, compensating signals are formed. They control the correct work of the motor. The feedback is made of an optical encoder, which is mechanically connected with the motor [1].

## 4. CONCLUSION

In the present article a system for positional control of a DC motor is presented. The system is distinguished with simplicity and low cost. The used language for description is VHDL, and the software is Xilinx ISE. The design was implement in SpatranII 100 by Xilinx.

## 5. REFERENCES

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