SIGMA-DELTA MODULATOR PROTOTYPING USING FPAA

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The paper presents the results from sigma-delta modulator prototyping. It briefly describes the classic structure of first and second order sigma-delta modulators. Three circuits of first order sigma-delta modulators and one circuit of a second order sigma-delta modulator were designed using Field Programmable Analog Array (FPAA). Their operation was examined in time domain at different constant input voltages and at sinewave input signal. The circuits were practically implemented and experimented by means of Evalution Board AN221E04 – a product of Anadigm Inc. The obtained results confirm the effectiveness of the designed prototypes. The proposed sigma-delta modulators can be applied in research and educational practice for designing programmable SC circuits and FPAA-based systems.

Keywords: Sigma-delta modulator, Field Programmable Analog Array (FPAA), Time-domain analysis, A/D and D/A converters, Switched capacitor, SC circuits

1. INTRODUCTION

The sigma-delta (Σ-Δ) modulator is the basis of the contemporary oversampling analog-to-digital and digital-to-analog converters. This type of circuit is very appropriate for high-resolution medium-to-low speed applications such as high quality digital audio, high-precision measurement devices, communication systems, etc. These devices utilize the only low cost conversion method, which provides both high dynamic range and flexibility in converting low-bandwidth input signal.

The above-mentioned fact is the reason for the big interest among the microelectronic circuit designers in the operation and practical implementation of the sigma-delta modulators [1].

With the aim of understanding the operation principle, it is especially useful to propose appropriate prototypes of first and second order sigma-delta modulators. These prototypes should be quick-realizable and should allow easy and simple alteration of the circuit configuration, as well as of the circuit elements' parameters. This would make possible a fast and effective analysis of the designed circuit operation, and a control of the relation between the elements' parameters and the circuit's mode of operation.

Field Programmable Analog Arrays (FPAAs), produced by Anadigm Inc., are modern programmable integrated circuits for analog and mixed signals processing. They are based on SC circuitry. This technology ensures high precise implementation of time constants and gain factors of the used analog functional blocks [2].

The process of designing of FPAA circuits is assisted by specialized CAD software – AnadigmDesigner2, which uses a library of configurable analog blocks – amplifiers, filters, multipliers, comparators, etc. From this viewpoint, the use of

FPAA is extremely appropriate as it is the most elegant, fastest and most perspective method for designing of analog prototypes. On the other hand, this would allow a quick transition to monolithic SC circuits (as custom-made or as a part of bigger integral circuits).

The paper presents the results from sigma-delta modulator prototyping. It describes the structure of first and second order sigma-delta modulators. Three circuits of first order sigma-delta modulators and one circuit of a second order sigma-delta modulator were designed. Their operation was examined in time domain at different constant input voltages and at sinewave input signal.

2. First and Second Order Sigma-Delta Modulator Block Diagrams

Fig.1 shows a simple block diagram of a first order sigma-delta modulator [1]. The feedback signal *r(n)* is subtracted from the input signal *Uin*. The difference *u(n)* accumulates in the integrator that feeds a comparator. The comparator is used as a one-bit quantizer, whose output *Uout* is also the output of the modulator. At the same time, the comparator controls one-bit digital-to-analog converter (D/A) that produces the feedback signal *r(n)*: when the D/A's input signal is "1", *r(n)* equals +*Uref*; when the D/A's input signal is "0", *r(n)* equals –*Uref.*

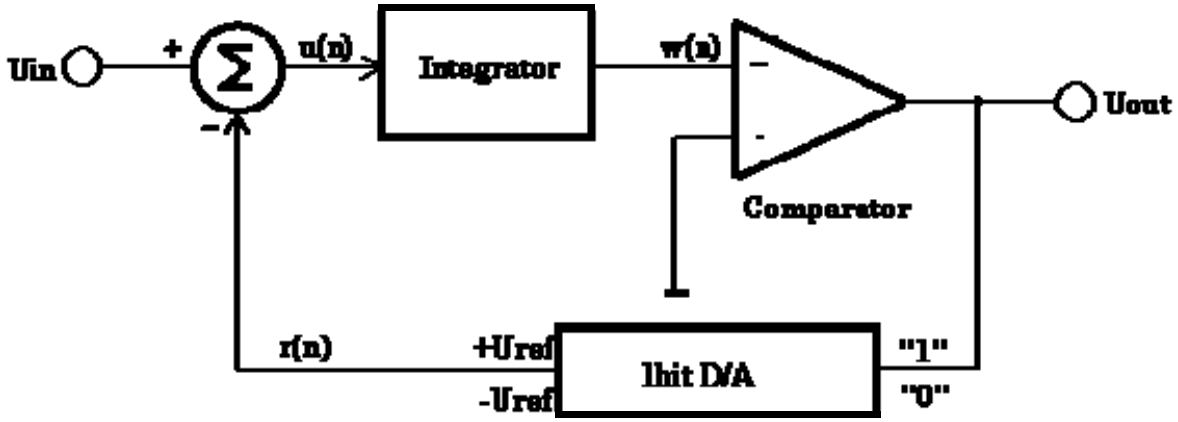

Fig.1 . First order sigma-delta modulator block diagram

When *Uin* is positive, the circuit operates as follows: when the output voltage of the integrator is smaller than zero, on the next step its value increases with the sum of the input *Uin* and reference *Uref* voltages. After that the output voltage decreases gradually with the difference between *Uref* and *Uin* voltages until its value becomes equal or smaller than zero. Then the described cycle repeats again.

Fig.2 shows a simple block diagram of a second order sigma-delta modulator. In this case the summator-integrator structure is repeated twice. The feedback signal *r(n)* is subtracted from the input signal *Uin*, and the difference accumulates in Integrator1. The difference between the output signal *w1(n)* of Intergator1 and the feedback signal *r(n)* accumulates in Integrator2 that feeds a comparator. The comparator is used as a one-bit quantizer, whose output *Uout* is also the output of the modulator. At the same time, the comparator controls one-bit digital-to-analog converter that produces the feedback signal *r(n)*.

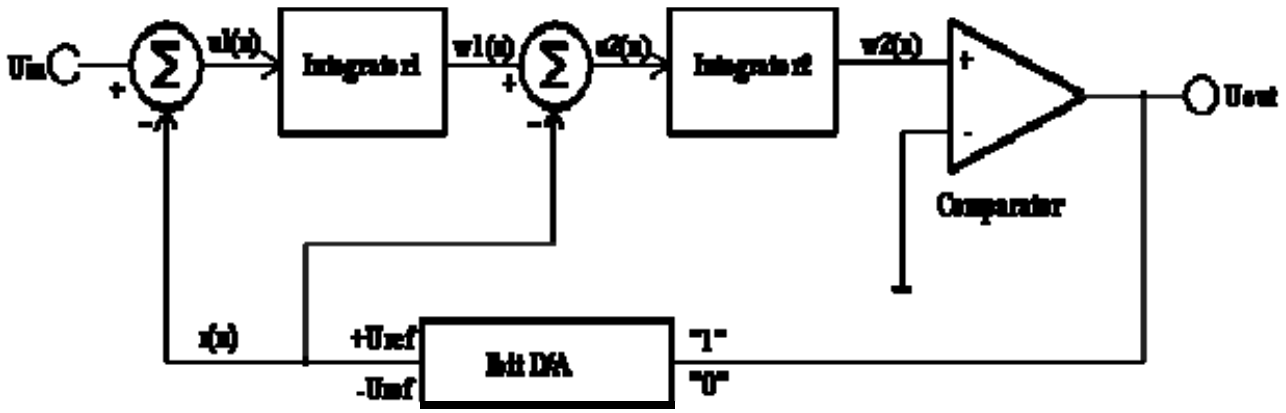

Fig.2 . Second order sigma-delta modulator block diagram.

3. FPAA IMPLEMENTATION

Anadigm Inc.'s FPAA has a very rich library of configurable analog modules (CAMs). This offers opportunities for various realizations of sigma-delta modulators.

Fig. 3 shows the implementation of the first order sigma-delta modulator by using the chip AN221E04, produced by Anadigm Inc. AnadigmDesigner2 program was used, which ensures the drawing, editing and simulating the circuit.

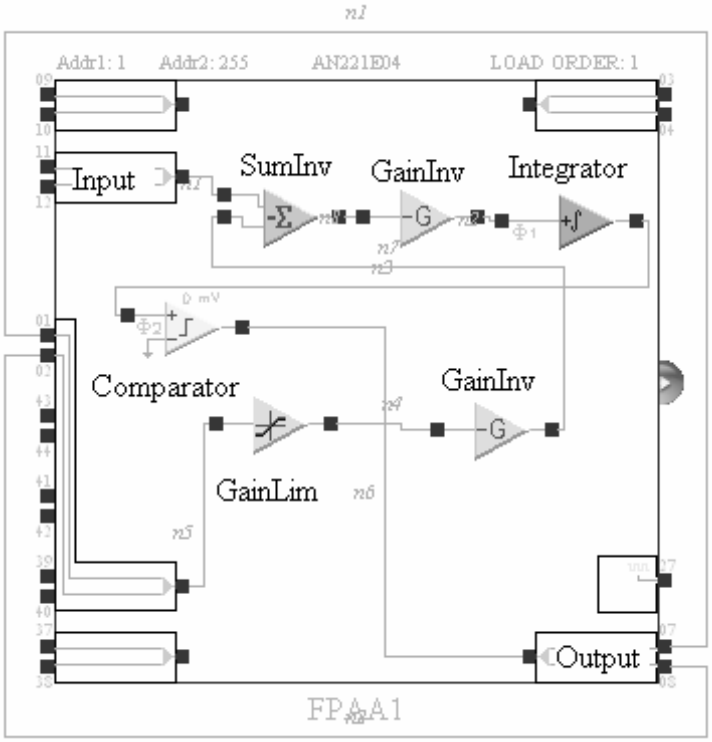

Fig. 3. FPAA implementation of first order sigma-delta modulator

The following CAMs were used for realization of the circuit: inverting summator (SumInv), noninverting integrator (Integrator), Comparator and amplifier with limiting output signal (GainLim). GainLim actually acts as a source of reference voltage *Uref*. Two inverting amplifiers (GainInv) were additionally included for the correct realization of the described operation.

On Fig.4 are given time diagrams in different points of the circuit, illustrating its operation at *Uin* = 0.5*V* and *Uref* = 1*V*. It can be observed that the output voltage of the integrator decreases in a stepwise fashion. The value of the input voltage is determined by the formula [1]:

$$U_{in} = \frac{m - n}{m + n} U_{ref} = \frac{3 - 1}{3 + 1} 1V = 0.5V, \quad (1)$$

where m is number of clock pulses at high *Uout* levels ("1") and n is number of clock pulses at low *Uout* levels ("0").

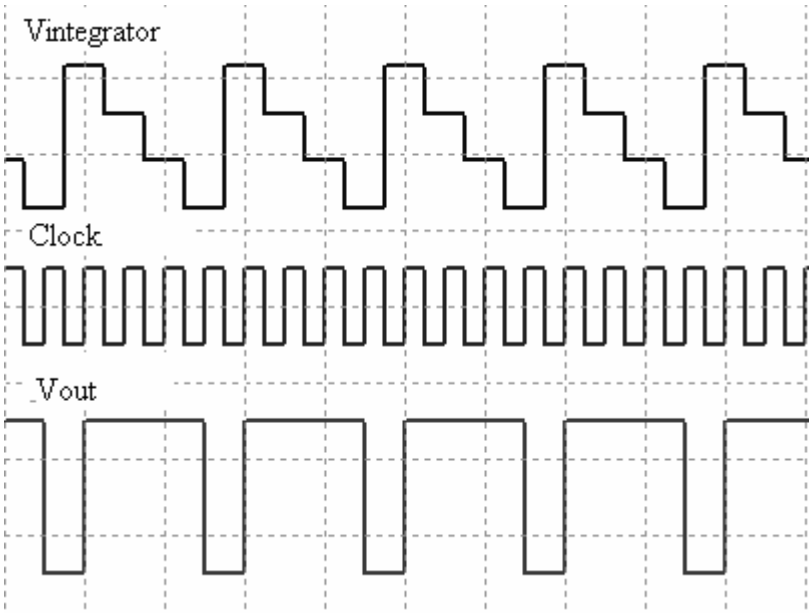

Fig.4. Time diagrams for the circuit shown on Fig. 3.

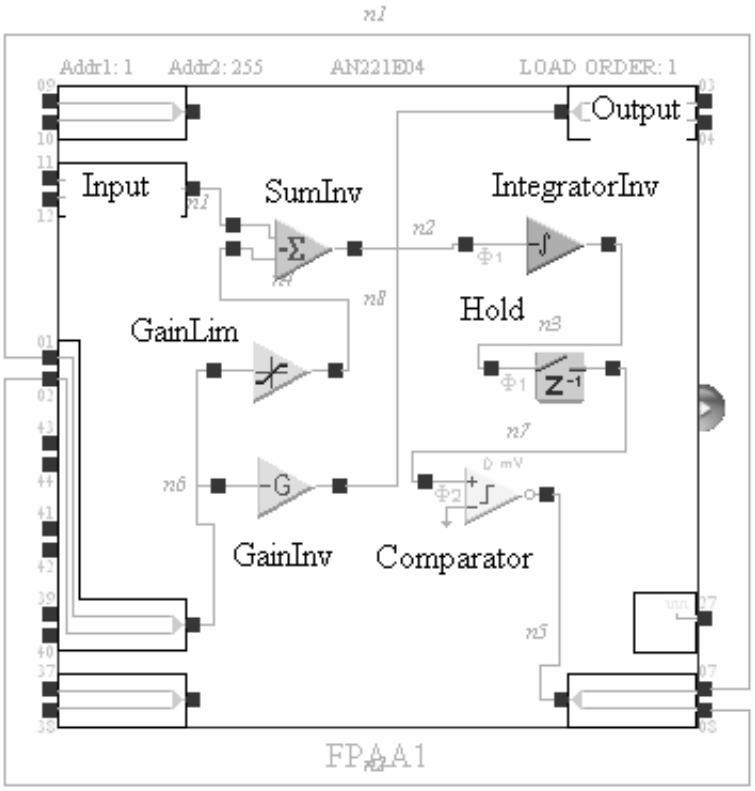

Fig.5. First order Σ–Δ modulator with Inverting Integrator

Fig. 5 shows a second version of a first order sigma-delta modulator designed by FPAA. In this case is used an inverting integrator (IntegratorInv), which allows the use of only one inverting amplifier (GainInv). In practice, the circuit is able to operate even without it, if the input voltage is determined by the formula:

$$U_{in} = \frac{n - m}{n + m} U_{ref}. \qquad (2)$$

A Hold circuit was additionally included in order to avoid operation with zero delay in the feedback circuit.

On Fig.6 are given time diagrams illustrating the circuit operation at *Uin* = 0.2*V* and *Uref* = 1*V*. For determining the value of the input voltage, it is necessary to use two consecutive high ("1") and low ("0") values of the output voltage: m = 2+1 = 3; n = 1+1 = 2.

In the Anadigm's CAM library is also present a summing integrator block (SumIntegrator). This makes possible the implementation of a third version of first order Σ–Δ modulator, using FPAA, by joining the first two blocks of the classic structure (Fig.1). The respective circuit is shown on Fig.7, and the time diagrams illustrating its operation at *Uin* = 0.125*V* and *Uref* = 1*V* are shown on Fig.8. In this version, a smaller part of the FPAA resources is

used due to the more economical realization of the circuit, which leads to a decrease in the consumed power.

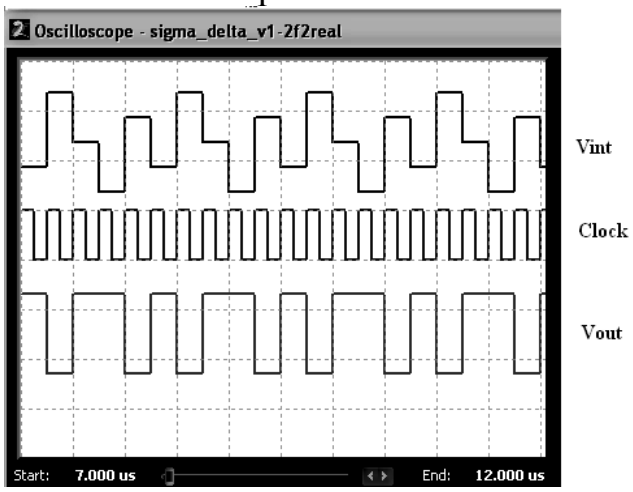

Fig.6. Time diagrams for the circuit on Fig. 5.

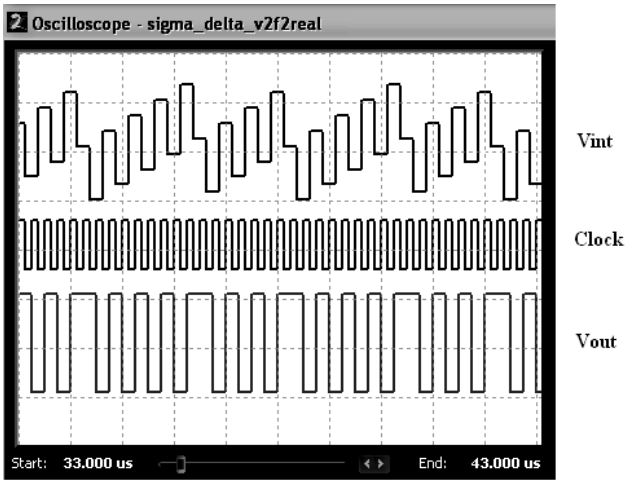

Fig.8. Time diagrams for the circuit on Fig. 7.

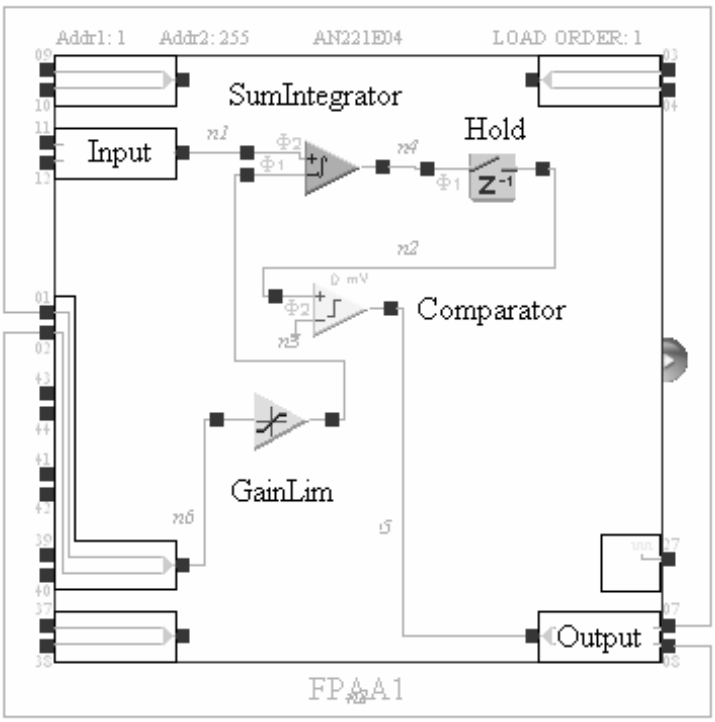

Fig.7. First order Σ–Δ modulator with Summing Integrator

For the designing of a second order Σ–Δ modulator is used the classic structure from fig. 2, and the circuit of a first order Σ–Δ modulator from Fig.7. The synthesized circuit in shown on Fig.9, and the time diagrams illustrating its operation at $Uin = 0.8V$ and $Uref = 1V$ – on Fig.10.

Very often a sinewave input signal is used for demonstration of the Σ–Δ modulator operation. Fig.11 shows time diagrams illustrating the operation of the circuit from Fig.7 at sinewave input signal with amplitude of $0.6V$ and a frequency of 20 kHz.

4. EXPERIMENTAL RESULTS

The operation of all proposed Σ–Δ modulator prototypes, using FPAA, was analysed at different *Uin* values, and the results are shown in Table 1.

5. CONCLUSIONS

The paper presents the results from sigma-delta modulator prototyping. It describes the structure of first and second order sigma-delta modulators. Three circuits of first order sigma-delta modulators and one circuit of a second order sigma-

delta modulator were designed. Using the CAD system AnadigmDesigner2, the FPAA circuits of the sigma-delta modulators were designed and simulated. The circuits were practically implemented and experimented by means of Evalution Board AN221E04 – a product of Anadigm Inc. Their operation was examined in time domain at different constant input voltages and at sinewave input signal. The obtained results confirm the effectiveness of the designed prototypes.

The obtained results confirm the effectiveness of the designed prototypes. The proposed sigma-delta modulators can be applied in research and educational practice for designing programmable SC circuits and FPAA-based systems.

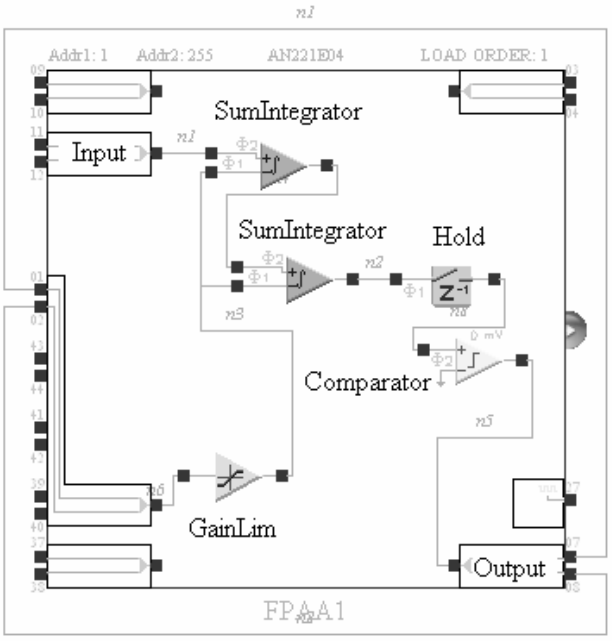

Fig.9. Second orrder Σ–Δ modulator

Uin	Uref	m	n
0.1	1	11	9
0.2	1	3	2
0.3	1	13	7
0.4	1	7	3
0.5	1	3	1
0.6	1	4	1
0.7	1	17	3
0.8	1	9	1
0.9	1	19	1

Uin	Uref	m	n
-0.1	1	9	11
-0.2	1	2	3
-0.3	1	7	13
-0.4	1	3	7
-0.5	1	1	3
-0.6	1	1	4
-0.7	1	3	17
-0.8	1	1	9
-0.9	1	1	19

Table 1

Operation of Σ–Δ modulator at different *Uin*

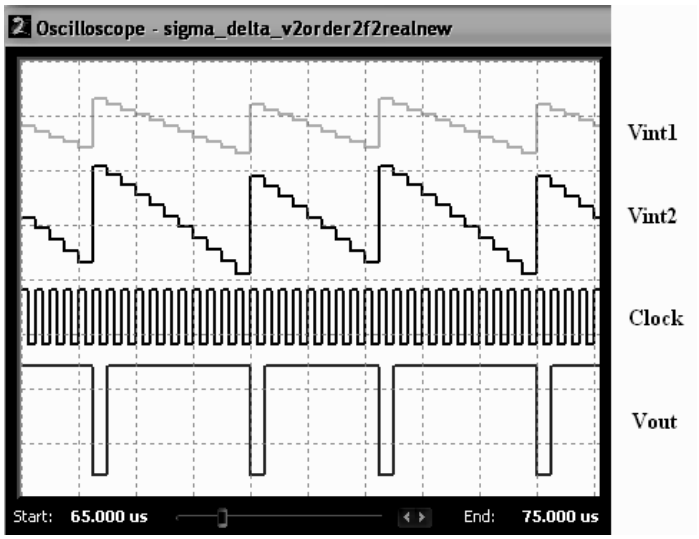

Fig.10. Time diagrams for the circuit on Fig. 9

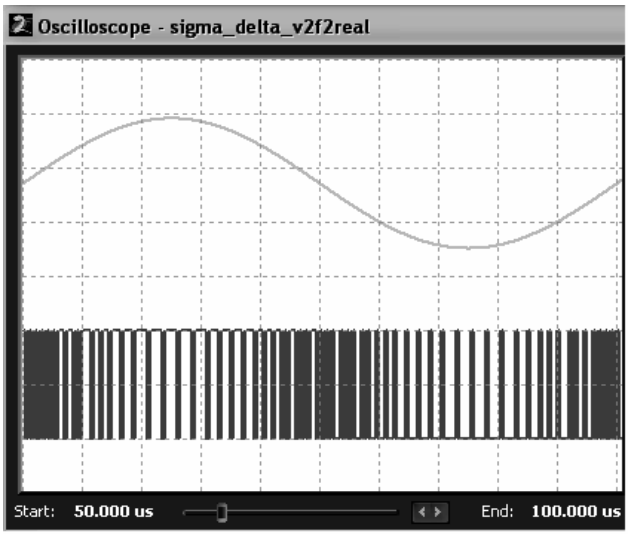

Fig.11. Time diagrams for sinewave Uin

6. REFERENCES

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[2] www.anadigm.com *Technical documentation*. Anadigm Inc.