MODELING AND IMPLEMENTATION OF FIRST ORDER SIGMA-DELTA MODULATOR

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Sigma-delta (∑Δ) modulation has become an increasingly popular choice for robust and inexpensive analog-to-digital and digital-to-analog conversion for the past years. As a result of this, the converters based on 1-bit ∑Δ modulators are widely used in different applications.

In this paper we present an experimental electronic realization of a first order Sigma-delta modulator. The schematic is simulated by use of PSpice and there is a good coincidence between the simulated and measured results. It will be used in laboratory practice on Theoretical Electrical Engineering (TEE).

Keywords: Sigma-delta modulators, PSpice.

1. INTRODUCTION

The sigma-delta modulation technique was first considered in around 1975 in Japan [1], [2]. However, its advantages have only been realized in recent years as high accuracy, 20-bit and beyond, conversion has become available.

The structure of basic sigma-delta modulator is shown in Fig.1, and consists of filter with transfer function G (z) followed by a one-bit quantizer in a feedback loop.

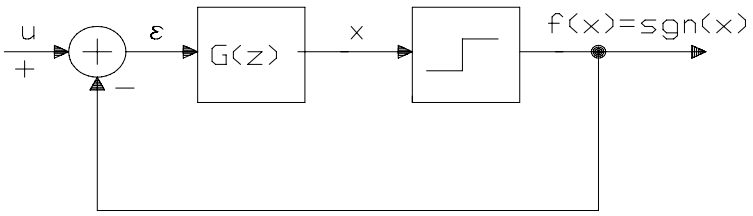

Fig. 1

Sigma-delta modulators are mainly used for analog to digital (A/D) and digital to analog (D/A) conversion of signals. The main difference to a conventional A/D converter is that ∑Δ converters trade off sampling rate with amplitude resolution [3]. This means that they sample at very high rates but only need one bit of amplitude resolution. The advantage is that they trade reduced analogue circuit requirements for increased digital circuit complexity. They only require a single bit A/D and D/A converter with a relatively inaccurate analogue integrator. These are simple analogue circuits, unlike those in conventional A/D converters, and are therefore easily implemented in VLSI circuitry. Because the ∑Δ modulator uses very high sampling rates, a simple RC-filter is adequate to prevent aliasing. The input filter can pass

frequencies many times higher than the frequencies of interest before filter cut-off is required. The need for abrupt cut-offs in recovery filters is also eliminated.

There is an ever-growing list of applications of the sigma-delta modulator. Among the most common are high performance audio, image processing, communications and specialized instrumentation.

The aim of this paper is to present an electronic implementation of a sigma-delta modulator and to compare the measurement results with the results obtained via simulation by PSpice. Further the schematic will be introduced in the laboratory practice on TEE. The paper is organized as follows. In the next section we give a theoretical background of sigma-delta modulation. Then in Section 3 we present the PSpice model of the modulator and the corresponding electronic scheme. Simulation and measurement results are compared and show good coincidence. The conclusions are given in Section 4.

2. THEORETICAL CONCEPTS OF SIGMA-DELTA MODULATION

2.1 Sampling of an analogue signal

Samples of an analogue signal are taken at equidistant time intervals. The frequency of these samples is the sampling frequency f_s. The Nyquist criterion states that the sample frequency must be at least two times the signal bandwidth f_b, to make recovery of the signal possible. Sampling at the Nyquist frequency f_{nyq}, means sampling at two times the signal bandwidth. With this sampling frequency the base band and side bands will be separated as shown in Fig. 2. Under-sampling is when $f_s < f_{nyq}$. In this case the side bands overlap the base band so recovery is not possible. This disturbance is called aliasing. Over-sampling is when $f_s > f_{nyq}$. In this case the side bands are spread further apart making recovery of the base band easier. This is because only a low cost recovery filter with a gradual cut off frequency is required to recover the signal. Fig. 3 illustrates under-sampling and over-sampling. Here the over-sampling ratio D, is the number of times the sampling frequency is greater than the Nyquist frequency: $D = \frac{f_s}{f_{nyq}} = \frac{f_s}{2f_b}$

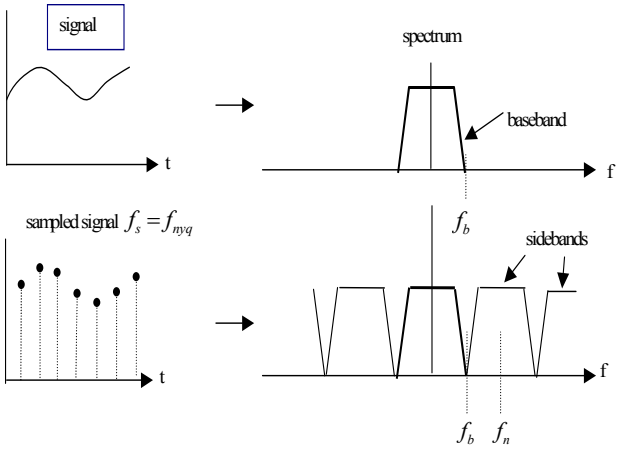

Fig. 2

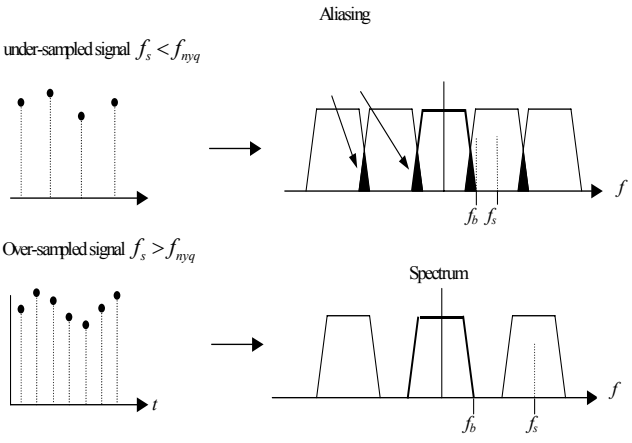

Fig. 3

2.2 Quantization of an analogue signal

When an analogue signal is quantized, its continuous amplitude value is rounded to a certain discrete amplitude value. These discrete values are the output quantization levels of the quantizer, which have a separation of q. The transfer characteristics of a quantizer can be seen in Fig. 4. The analogue signal $\sigma(t)$, is rounded to its nearest quantization output level $y(t)$. This introduces a quantization error $e_q(t)$, which varies between $+q/2$ and $-q/2$. This process is a non-linear operation that is effected when a physical quantity is represented numerically. Incorporation of such a process within a circuit makes the entire system non-linear and difficult to calculate.

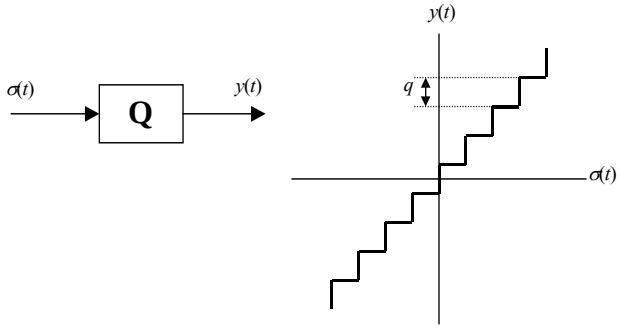

Fig. 4

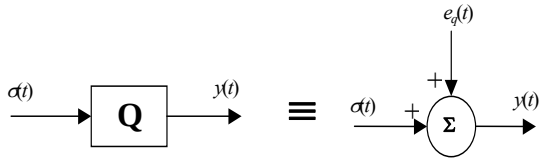

Fig. 5

In systems where the input signals fluctuate sufficiently and quantization takes place over a long period of time, the error $e_q(t)$ can be thought of as white noise. The white noise or quantization noise is spread uniformly over all frequencies and there is a uniform distribution of error over an interval of $+q/2$ and $-q/2$. The average of this error is zero but the power of this quantization noise is $\overline{e_q(t)^2} = \frac{q^2}{12}$.

As the quantizer can be thought of as introducing quantization noise, it can be modeled as a unity gain error source as shown in Fig. 5. By using this model noise calculations are made possible and the r.m.s. amplitude of the noise signal is

$$e_q(t) = \sqrt{\frac{q^2}{12}}\ .$$

2.3 Model for a Sigma-Delta modulator

In Fig. 6 a model for a single bit first order sigma-delta modulator is shown [4].

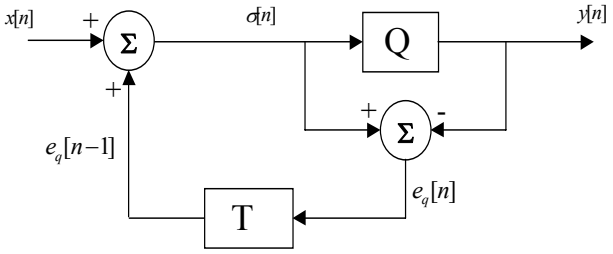

Fig. 6

The quantization error $e_q[n]$ is fed back and summed with the input. By subtracting the error signal from the input signal gives an average error in the output signal of zero. This is where the function of a sigma-delta modulator excels that of

conventional A/D converters. The feedback causes noise shaping. Q is a 1-bit quantizer, which produces a 1-bit data word for each sample. Note that there is no D/A converter in the feedback loop that sums up with the analogue input signal. This is due to the two quantization levels, with values V+ and V-. It would introduce no error, so its analogue output signal contains the same information as its digital input signal. **T** is a time delay that must be present in the loop back to the input. The summing junctions are denoted by **Σ**. [*n*] indicates a step in time, i.e., *n*=1,2,3,4, etc. In other words, time has discrete values.

The way in which a sigma-delta modulator converts an input signal into a digital output signal is explained by using a DC input signal but the theory also applies to an AC signal. The feedback loop in the model forms a servo function that tends to drive $\sigma[n]$ toward zero. The system tries to minimize the error between its input and output, which gives rise to such a variation in $y[n]$ that it is average value will approximate the input signal over time.

It should be noted that the range of $x[n]$ must be less than or equal to the output range of the quantizer, because if $x[n]$ exceeds this range, the system overloads because it cannot correct itself anymore.

3. Model of the Schematic Implementation of a First Order Sigma-Delta Modulator and PSpice Simulations.

In [4] we have presented the first order sigma-delta modulator scheme given in Fig. 7. On this figure a PSpice model is plotted with all the elements used in its realization. The circuitry accepts AC or DC analog input sources and gives digital output signal. For testing and verification of the simulated circuitry model DC input signals from range from 0 to 2.5V that makes the range from 0 to 1 has been applied to the scheme.

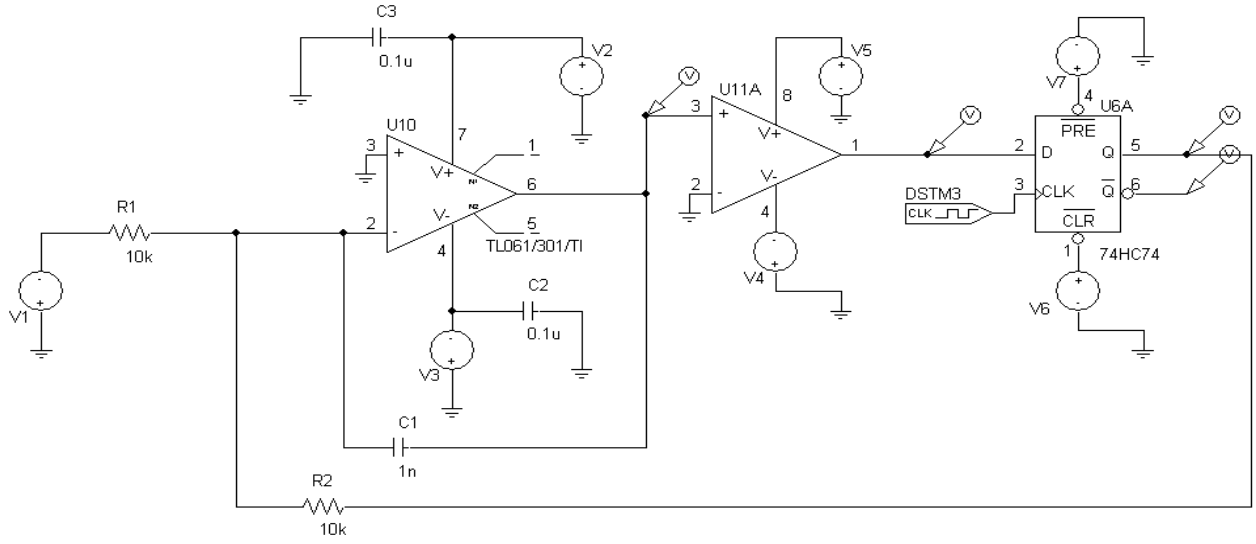

Fig. 7

For the PSpice [5] and electronic model realization the following elements have been used: TL061 is a low power j-fet operational amplifier which in this case as it is connected and used in scheme plays the role of an analogue integrator, while the

LM9203 element is a low power low offset voltage comparator. The 74HC74 element is a D-type positive edge triggered flip flop with clear and preset. The other elements are regular DC voltage sources, resistors and capacitors. Digital synchronization clock is used for the 74HC74 part and all the obtained results are gained when applying 100KHz clock signal. Modulator's input should be scaled to 0 to 1 from the active range from 0V to 2.5V. During the simulations done with PSpice we observed that the region of input signals that guarantee modulator's stability is between 0.25V to 2.25V – in this case when scaled down input signals lower than 0.1 and higher than 0.9 lead our modulator to instability. In the following figures the modulator's behavior is depicted with probe. The resulting output of the analog integrator in the PSpice realization of our sigma-delta modulator is plotted in Fig. 8, while in Fig.9 the resulting output of the comparator and the Q output of 74HC74's are given.

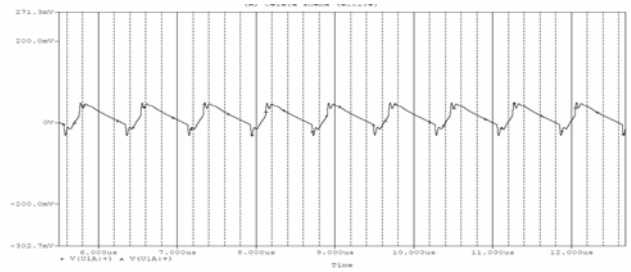

Fig. 8

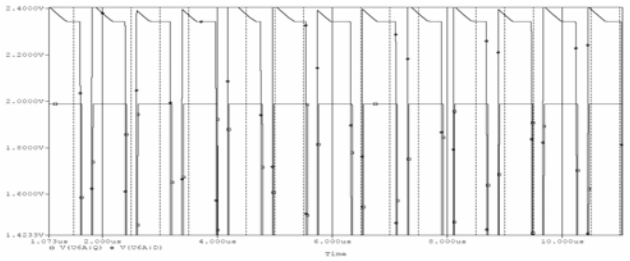

Fig. 9

The feed from our digital clock impulse generator used for 74HC74 flip-flop is depicted in Fig. 10 while in Fig. 11 the resulting outputs of the 74HC74's (digital presentation of the signal) are shown.

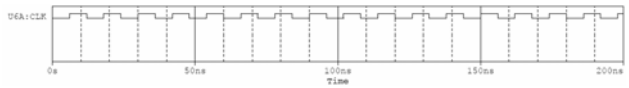

Fig. 10

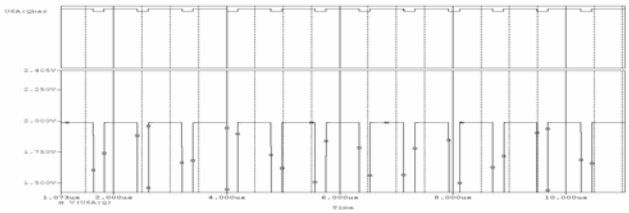

Fig. 11

Based on PSpice model considered, we created an electronic model realization - printed circuit board (PCB) given in Fig. 12. We utilize the same elements that we used in the PSpice model. The whole laboratory setup with the designed PCB, DC sources, oscilloscope, etc. is shown in Fig. 13. The output of the analog integrator viewed on oscilloscope is given in Fig. 14 and the digital output signal observed on oscilloscope can be seen in Fig.15.

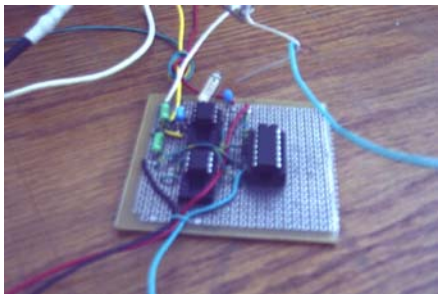

Fig. 12

Fig. 13

The obtained results are almost identical with the results obtained from PSpice simulations which lead us to the conclusion that the schematic is working properly and in the electronic model when changing the input in real-time, the appropriate changes in modulator's output simultaneously are occurring.

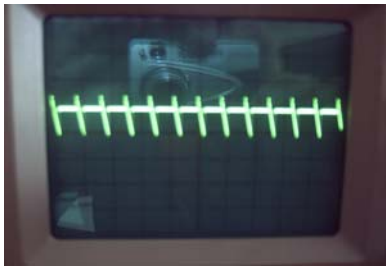

Fig. 14

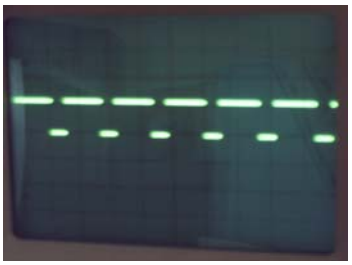

Fig. 15

4. CONCLUSION

The electronic realization of the first order sigma-delta modulator presented appeared to be working fine and without problems, which make it ready for future incorporation within the laboratory practice of TEE. Focus for some future experimental work will be the extension of modulator's model to higher order.

5. ACKNOWLEDGMENT

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6. REFERENCES

[1] J. C. Candy, G. C. Temes, *Oversampling Delta-Sigma Data Converters*, IEEE Press, 1992, New York.

[2] S. R. Norsworthy, R. Schreier, G. C. Temes, *Delta-Sigma Data Converters*, *Theory, Design and Simulation*, IEEE Press, 1997, New York.

[3] R. M. Gray, *Oversampled sigma-delta modulation*, IEEE Trans. Commun., 35, pp. 481-489, 1987.

[4] G. Tsenov, V. Mladenov, *Modeling, simulation and implementation of sigma delta modulators*, will appear in the Proc. of the Fourth International Conference on Challenges in Higher Education and Research in the 21 Century, Sozopol, 2006.

[5] PSpice Schematics "User's guide" 1985-2000, Cadence Design Systems, Inc.