AN ENHANCED SIMULATION MACROMODEL FOR CURRENT-FEEDBACK AMPLIFIERS

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In this paper, an enhanced SPICE macromodel for Current-Feedback Amplifiers (CFA) is presented which takes into account the second-order effects such as the noise, the common-mode rejection ratio (CMRR), the positive and negative output voltage swing, and power-supply rejection ratio (PSRR) as a function of temperature. The simulation model is developped through modifying the basic macromodel employing the mechanism of controlled sources and subcircuits. Model parameters are extracted for the integrated CFA AD8001 as an example. The accuracy of the model is demonstrated by comparison between the data sheet parameters of the real IC and the simulation results.

Keywords: analogue circuits, current-feedback amplifier, SPICE, Modelling.

1. INTRODUCTION

The current-feedback amplifiers (CFAs) as a variety of op amps, has been realized to overcome the finite gain-bandwidth product of the conventional VFA (Voltage Feedback Amplifiers). The CFAs can provide not only higher bandwidth than the VFA based circuits, but also a high slew rate capability. Moreover, the CFAs have a build-in voltage buffer, so it does not need additional buffers compared with the current-conveyor-based circuits. Thus, there are benefits in using CFAs as basic blocks to realize various analogue signal processing circuits.

Several CFA macromodels have been developed and reported in the literature [1-5]. The macromodel due to Bowers, Alexander and Buxton [1] includes more common small-signal effects such as small-signal transient and frequency response but ignores the most of the second-order effects such as noise, PSRR, temperature effects, etc. There is another CFA macromodel [2] developed by National Semiconductor, which simulates the more common small-signal effects, as well as temperature effects, noise and PSRR. Also modelled are large-signal effects, such as non-linear input transfer characteristics and input (output) slew rate limiting. This model does not simulate asymmetrical values of the maximum output voltage and the temperature drifts for the CMRR, the PSRR and the maximum output voltage. Recently, two linear, frequency-dependent macromodels for the CFA were proposed for analogue/digital (mixed-mode) simulation [3]. Both macromodels simulate the actual performance of typical CFAs for a wide range of frequencies but not includes the temperature dependencies of the main electrical parameters and the noise effects. In Ref. [4, 5] the CFA models proposed by Texas Instruments and National Semiconductor are not the macromodels, but rather a simplified circuit model at the transistor level. These models produce the most accurate simulation results, but because of the complexity, require longer simulation time. There are suitable only for

special purpose applications. The objective of developing the model presented here is to analyze and modelled second-order effects of the real CFAs.

2. MACROMODEL DEVELOPMENT

The schematic diagram of the improved input stage for the CFA macromodel is shown in Fig. 1. It is based on a previous SPICE macromodel [1], with the additional

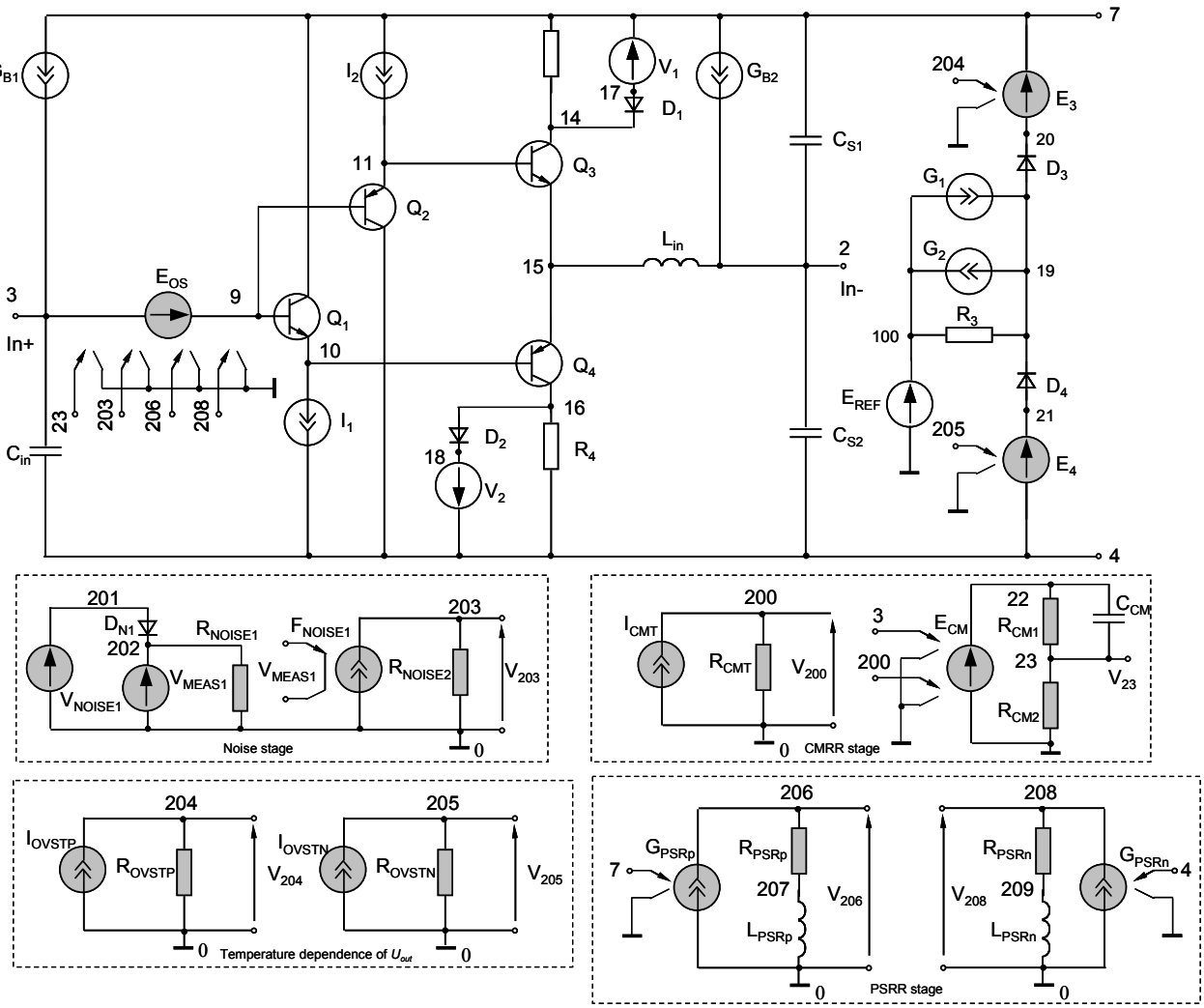

Fig. 1. Complete equivalent circuit of the input stage for the proposed CFA macromodel.

capability to simulate the CMRR, the PSRR and the output voltage swing versus temperature, as well as noise effects. In Fig. 1 the new elements and stages, added to the input stage are marked in grey.

Various parameters have been modelled as follows.

2.1. Modelling of the CMRR as a function of temperature

The temperature dependence of the CMRR is modelled by adding new elements and temperature stage to the equivalent circuit of the existing macromodel for the CFAs. As it shown in Fig. 1, a voltage-controlled voltage source (VCVS) E_{CM} from the original equivalent circuit connected between node 22 and 0 is replaced with linear 2-port VCVS (marked in grey, see Fig. 1). The state of node 22 will have to

follow the change in the input common-mode voltage and the ambient temperature, modelling CMRR. The temperature dependence of the CMRR is modelled by additionally defined temperature stage consisting ideal current source I_{CMT} and SPICE temperature dependent resistor R_{CMT}, which is controlled with equation [6]:

$$R_{CMT}(T) = R_{CMT0}\left[1 + TC1(T - T_{nom}) + TC2(T - T_{nom})^2\right], \quad (1)$$

where R_{CMT0} is the value of the resistor at $T_{nom} = 27°C$ (SPICE-Option TNOM), T is the temperature in $°C$, $TC1$ is the linear temperature coefficient and $TC2$ is the quadratic temperature coefficient. The voltage $V_{200,0}$ works as a quadratic temperature controlled input value for VCVS E_{CM} in the model, i.e. $V(E_{CMT}) = k_{CMT}V_{3,100}V_{200,0} = = k_{CMT}V_{3,100}I_{CMT}R_{CMT}(T)$, where $k_{CMT}\left[V^{-1}\right]$ is a linear coefficient and $V_{3,100}$ is the input common-mode voltage. Then the CMRR of the simulation model can be found by

$$CMRR = k_{1,EOS}\frac{R_{CM2}}{R_{CM1} + R_{CM2}}k_{CMT}I_{CMT}R_{CMTT0}\left[1 + TC1(T - T_{nom}) + TC2(T - T_{nom})^2\right] \quad (2)$$

The temperature coefficients $TC1$ and $TC2$, and the resistance R_{CMTT0} from Eq. (2) can be calculated by employing the least squares sense technique.

2.2. Modelling the noise voltage spectral density effects

The approach used for improving the noise effects modelling to any macromodel of analogue integrated circuit is similar to the techniques used for input offset voltage [2]. As it is shown in Fig. 1, the equivalent circuit of the existing macromodel has been modified by adding noise generators that simulate the thermal (white) noise and 1/f noise (Flicker noise) of an actual CFA. The polynomial VCVS E_{OS} reflects the error voltage from the additionally defined noise stage. The noise stage of the model consist two independent sources V_{NOISE1} and V_{MEAS1}, one diode D_{N1} to produce 1/f noise, two resistors R_{NOISE1} and R_{NOISE2}, and a ideal current-controlled current source (CCCS) F_{NOISE1}. The voltage source V_{NOISE1} determines the voltage at node 201. Its value is fixed at 0,61V to provide a forward voltage drop across D_{N1}. Role of the resistor R_{NOISE1} is to generate white noise current. Flicker noise current is generated in the diode D_{N1}. The noise currents thus generated, $\bar{i}^2_{R_{NOISE1}}$ and $\bar{i}^2_{D_{N1}}$ are routed through a zero voltage source V_{MEAS1}, towards the ground. The combined noise current is monitored by CCCS F_{NOISE1} and appears as a voltage across the resistor R_{NOISE2}. The total rms noise signal that result at node 203 is the square root of the sum of the average mean-square value of the individual sources:

$$V_{203,0} = \sqrt{\bar{e}^2_{R_{NOISE1}} + \bar{e}^2_{D_{N1}}}\,. \quad (3)$$

where the $\bar{e}^2_{R_{NOISE1}} = k_{FNOISE}\bar{i}^2_{R_{NOISE1}}R^2_{NOISE2}$ is white mean-square voltage noise from R_{NOISE1} and $\bar{e}^2_{D_{N1}} = k_{FNOISE}\bar{i}^2_{D_{N1}}R^2_{NOISE2}$ – 1/f noise from diode D_{N1}. Signal generated at node 203 is used for forming the equation of the VCVS E_{OS} as follows:

$$V(E_{OS}) = k_{o,EOS} + k_{1,EOS}V_{23,0} + k_{2,EOS}V_{203,0}\,. \quad (4)$$

The coefficient $k_{2,EOS}$ is used for modelling the change in the offset voltage as a result of noise generation.

2.3. Modelling the maximum output voltage as a function of temperature

The temperature dependence of the output voltage swing is implemented by modifying the voltage limiting stage of the existing CFA macromodel. As it shown in Fig. 1, the independent voltage sources V_3 and V_4 from the original equivalent circuit connected between nodes 7, 20 and 21, 4 of the input stage are replaced with linear one-port VCVSs E_3 and E_4. The additionally defined temperature stages consists of two ideal current sources I_{OVSTP} and I_{OVSTN}, and two temperature-dependent resistors R_{OVSTP} and R_{OVSTN}. The desired output voltage limitation is provided by D_3, D_4, E_3 and E_4 in Fig. 1, and resistors $R_{o1} - R_{o2}$ in the output stage [1]. When a load R_L is connected to the output the required value of the $V(E_3)$ and $V(E_4)$ for a different temperature can be solved from the two linear equations as

$$V(E_3) = k_{1,E3}I_{OVSTP}R_{OVSTP}\left[1 + TC1(T - T_{nom}) + TC2(T - T_{nom})^2\right] = V_7 - V_{out}^{+}(R_L + R_{o1} \,||\, R_{o2})/R_L\,, \quad (5)$$

$$V(E_4) = k_{1,E4}I_{OVSTN}R_{OVSTN}\left[1 + TC1(T - T_{nom}) + TC2(T - T_{nom})^2\right] = V_4 - V_{out}^{-}(R_L + R_{o1} \,||\, R_{o2})/R_L\,, \quad (6)$$

The temperature coefficients and resistor values R_{OVSTP} and R_{OVSTN} at $T_{nom} = 27°C$ are calculated for the desired temperature behaviour.

2.4. Modelling the positive and negative PSRR as a function of temperature

The addition of ac PSRR, to any macromodel of analogue integrated circuit is similar to the techniques used for modelling CMRR and is based on those described in [2, 7]. The schematic diagram of the improved input stage with the PSRR effects approximated by one-pole transfer function is shown in Fig. 1. The third and fourth part of the offset voltage-source E_{OS} reflects the error voltages from the PSRR stages. The additionally defined PSRR stages simulating transfer function with one zero consists two VCCSs G_{PSRp} and G_{PSRn}, and frequency-dependent RL groups (R_{PSRp} - L_{PSRp} and R_{PSRn} - L_{PSRn}).

The temperature dependence of the PSRR is modelled by temperature-dependent resistors $R_{PSRp}(T)$ and $R_{PSRn}(T)$, which are controlled with the equation (1).

The positive $PSRR^{+}$ and negative $PSRR^{-}$ will be determined by the following expressions:

$$PSRR^{+} = \frac{GAIN}{GAIN_{PSR+}} = \frac{V_{OUT}/V_{9,3}}{V_{OUT}/(V^{+} \pm \Delta V^{+})} = \frac{\left(k_{1,GPSRp}R_{PSRp}(T)\right)^{-1}}{k_{3,EOS}\dfrac{L_{PSRp}}{R_{PSRp}(T)}\left(p + \dfrac{R_{PSRp}(T)}{L_{PSRp}}\right)} = \frac{H^{+}\omega_p^{+}}{p + \omega_p^{+}}\,, \quad (7a)$$

$$PSRR^{-}=\frac{GAIN}{GAIN_{PSR-}}=\frac{V_{OUT}/V_{9,3}}{V_{OUT}/\left(V^{-}\pm\Delta V^{-}\right)}=\frac{\left(k_{1,GPSRn}R_{PSRn}(T)\right)^{-1}}{k_{4,EOS}\dfrac{L_{PSRn}}{R_{PSRn}(T)}\left(p+\dfrac{R_{PSRn}(T)}{L_{PSRn}}\right)}=\frac{H^{-}\omega_{p}^{-}}{p+\omega_{p}^{-}},\quad (7b)$$

where $GAIN_{PSR+}=V_{OUT}/\left(V^{+}\pm\Delta V^{+}\right)$ and $GAIN_{PSR-}=V_{OUT}/\left(V^{-}\pm\Delta V^{-}\right)$ is the voltage gain of spikes (ΔV^{+} and ΔV^{-}) on the positive and negative power supply lines (V^{+} and V^{-}). Comparing the last expressions (7a) and (7b) leads to: $\omega_{p}^{+}=R_{PSRp}(T)/L_{PSR1}$ – pole of $PSRR^{+}$; $PSRR_{DC}^{+}(T)=H^{+}=1/k_{3,EOS}k_{1,GPSRp}R_{PSRp}(T)$ – positive dc PSRR; $\omega_{p}^{-}=R_{PSRn}(T)/L_{PSRn}$ – pole of $PSRR^{-}$; $PSRR_{DC}^{-}(T)=$ $=H^{-}=1/k_{4,EOS}k_{1,GPSRn}R_{PSRn}(T)$ – negative dc PSRR.

These relationships are of basic importance for the methodology of determining the model parameters of the equivalent circuit.

3. MACROMODEL PERFORMANCE

The verification of the macromodel (Fig. 1) improved with second-order effects are carried out by comparing simulation results with data sheet parameters of the integrated CFA AD8001 from Analog Devices [8]. The test circuits for simulation are created following the test conditions given in the manufacturer's data.

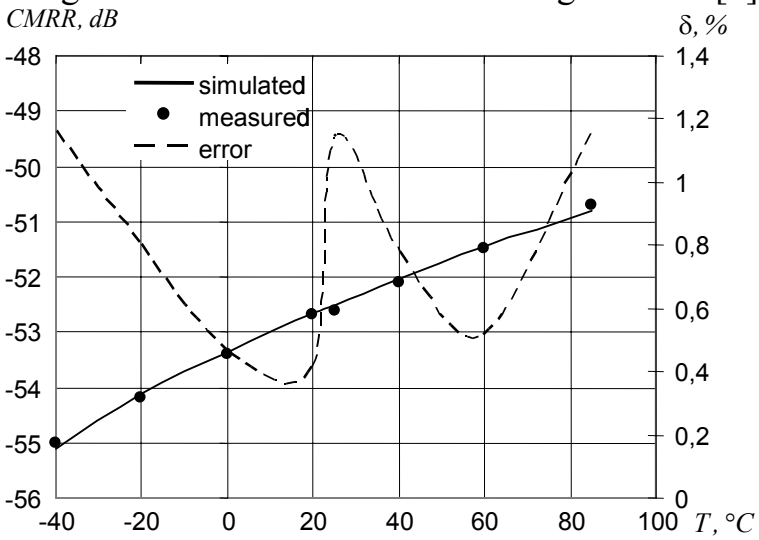

Fig. 2. Comparison of the manufacture's data and simulation results for the CMRR vs. temperature.

In Fig. 2 are presented simulation output (solid line), experimental results (data points plotted) for the *CMRR* and error in percents ($\delta,\%$) versus temperature. The comparison analysis shows that, the average error is not higher than 2%, which guarantees the sufficient degree of accuracy.

To calculate noise voltage versus frequency ac sweep and noise analysis is performed. The power supply voltages of the test circuit are chosen ±5V and the simulation is performed at temperature 25°C. Figure 3a and Figure 3b shows noise voltage spectral density of the real IC and the simulation output, respectively. Notice that the simulated white noise within the frequency range $\Delta f=100Hz-100kHz$ and Flicker noise voltage at the lowest frequency to $f_{min}=10Hz$ closely match that of the actual device ($\delta<5\%$).

Figure 4 shows the maximum output voltage versus temperature of the real AD8001 and simulation output. The test circuit for simulation includes one CFA macromodel connected as a non-inverting, unity-gain amplifier (voltage follower)

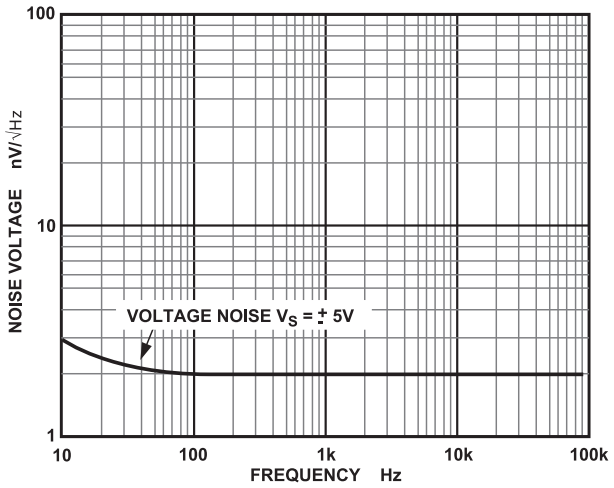

Fig. 3a. AD8001 noise voltage spectral density versus frequency.

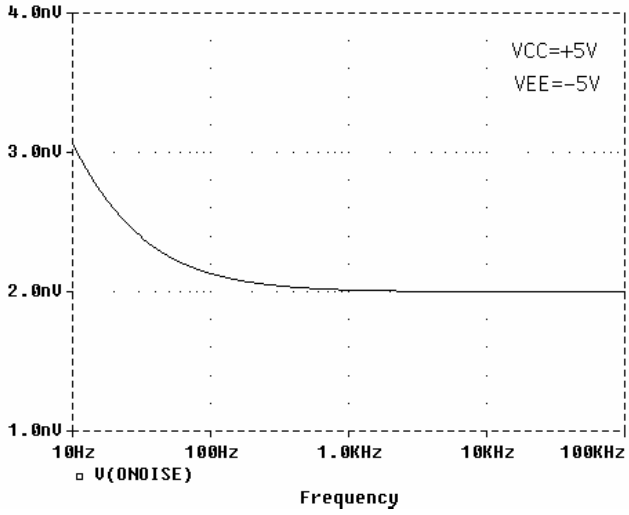

Fig. 3b. Simulated noise voltage spectral density versus frequency.

that has 50Ω input resistor, 1050Ω feedback resistor and are set ±5V supplies. The simulation testing is performed within temperature range from -40°C to +85°C. Also during the process of simulation is specified and performed dc sweep analysis with a level of the input voltage from –5V to +5V and for two load resistors $R_L = 50\Omega$ and $R_L = 150\Omega$.

The verification check of the ac *PSRRs* is performed for ±5V supplies and with the additionally defined small-signal sources connected is series to the supply

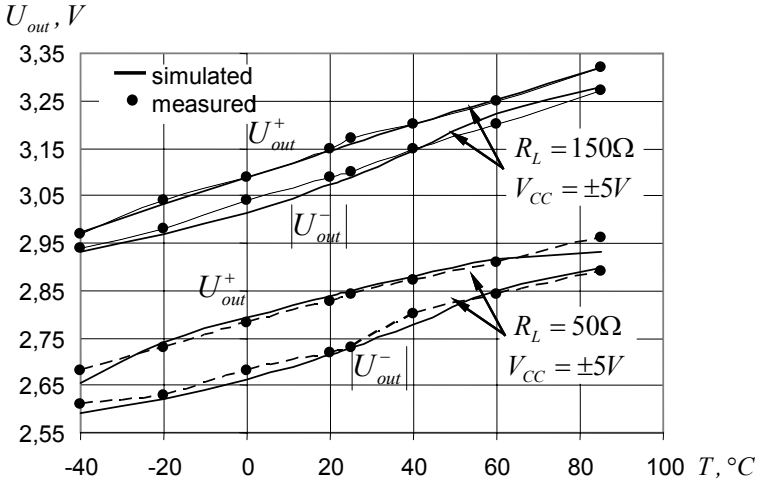

Fig. 4. Comparison of the manufacture's data and simulation results for the maximum output voltage vs. temperature.

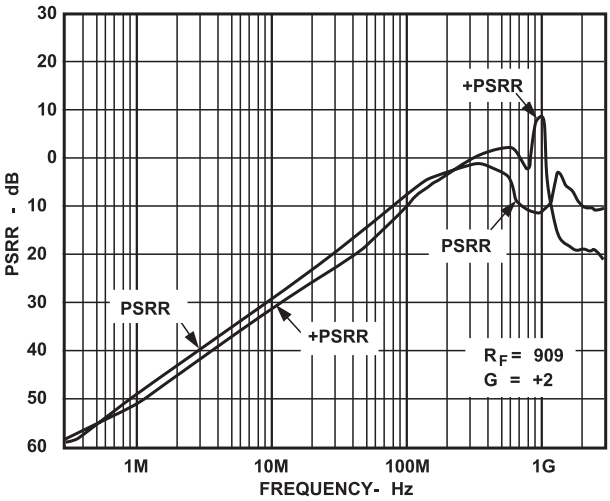

Fig. 5a. AD8001 PSRR versus frequency.

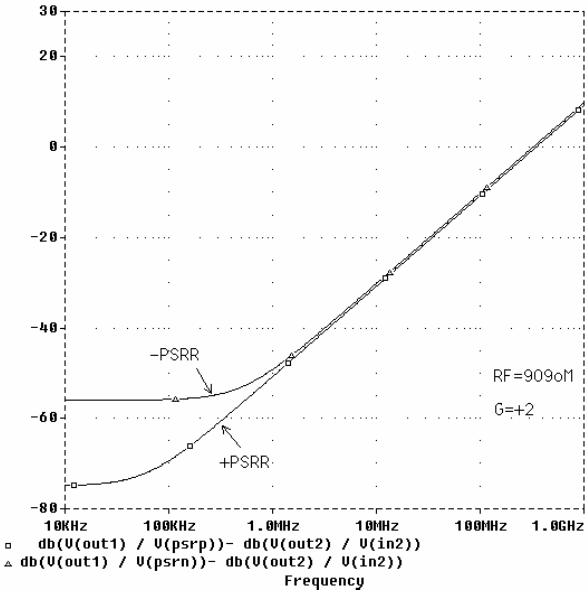

Fig. 5b. Simulated PSRR versus frequency.

voltages for emulating spikes on supply lines. Fig. 5a and 5b shows the ac *PSRR* logarithmic characteristics and simulation results at *T*=25°C. A good matching can be observed from the figures except at high frequency (above 100MHz) where the model is not very accurate, because the higher poles/zeros of the frequency response are not modelled. The verification check of the *PSRR* temperature effects is performed within temperature range from –40°C to +85°C. Simulation output and experimental results of the dc *PSRR* parameters in temperature range are given in Fig. 6.

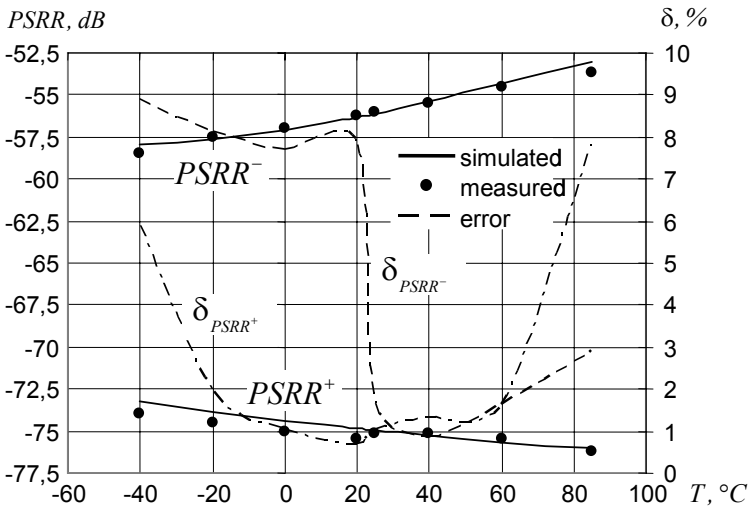

Fig. 6. Comparison of the manufacture's data and simulation results for the dc PSRR as a function of temperature.

4. CONCLUSIONS

An improved simulation model is presented, which takes into account a second-order effects for monolithic CFAs. The proposed model is independent from actual technical realizations and is based upon compromises regarding the representation of exact circuit structures in the model. The efficiency of the model was proved by comparison of simulation results and data sheet parameters of the CFA AD8001. Despite the addition of all these new features, the macromodel's simulation speed and computer resources needed are still equal to those of the SPICE standard libraries models. However, other CFAs, especially those using different topologies or technologies, may well exhibit different temperature functions of the electrical parameters. These matters are the subjects of further investigation.

5. REFERENCES

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