

LOW-VOLTAGE OPERATIONAL AMPLIFIERS FOR MIXED-SIGNAL APPLICATIONS

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This paper deals with problems encountered in the design of compact two-stage CMOS operational amplifiers, which operate on a single 3V supply voltage and are suitable for VLSI library cells. Various input and output stages are designed and compared with respect to their advantages and disadvantages. To ensure compatibility with the digital part and to keep production costs low, only the basic CMOS process modules are used. The paper also discusses the experimental results of several test chips containing a family of compact CMOS low-voltage opamps fabricated in 0.35 μ m double-poly, double-metal processes.

Keywords: CMOS IC, operational amplifier, low-voltage, mixed-signal

INTRODUCTION

The opamp is a fundamental component in analog and mixed-signal systems and its performance directly affects the performance of the entire system. The continuously decreasing supply voltage imposes great difficulties to the design of analog circuits in mixed-signal systems as the threshold voltages do not scale accordingly. It is, therefore, our goal to develop low voltage design methodologies and techniques.

With the supply voltages going down, rail-to-rail operation of analog circuits has become nearly mandatory so that a sufficient signal-to-noise ratio is achieved. The straightforward method for achieving a rail-to-rail input stage is to connect in parallel n-channel and p-channel differential pairs. It is highly desirable that the circuit performance is independent of the input common-mode (CM) voltage. The problem with the complementary input stages is that in the middle of the CM range, both the P and the N part operate and the total transconductance is twice as high as the value when the CM voltage is close to any of the rails and only one of the pairs operates.

The paper discusses problems encountered in the design of low-voltage compact two-stage CMOS operational amplifiers suitable for VLSI library cells.

OPAMP DESIGN

The two-stage opamps were given a preference since they allow simple and easy frequency compensation. Let us briefly consider the requirements to be met by the input and the output stages.

I. The input stage.

The performance of a good rail-to-rail input stage should be independent of the CM voltage applied. In regard to small-signal behavior, a constant transconductance g_m is of crucial importance; and in regard to large-signal behavior, a Slew Rate (SR) constant over the CM range is sought. These design goals should be achieved by means of robust circuits that do not rely on critical component values or strict device matching. Numerous solutions have been reported; some of the most popular are: keeping $I_P + I_N$ constant [1]; level shifters between the P- and N- gates [5]; current switches that steer I_P or I_N 4 times when only one of the pairs operate [8]; electronic zener diode [7] [8]; keeping $\sqrt{I_P} + \sqrt{I_N}$ constant [6]; minimum/maximum current selection [4].

The first approach is only effective if the MOS transistors work in weak inversion, hence the Gain BandWidth and the SR of the opamp are very low; in strong inversion a 40% increase of g_m in the middle of the common-mode range is introduced. Level shifters between the P- and N- stage are easy to implement; however, they are very sensitive to process variations and are characterized by increased input offset voltage. Current switching has found wide application due to its simplicity and low sensitivity to process variations. However, current switching significantly reduces the CMRR in the transition region; moreover, the SR is not constant over the full CM range. The electronic zener diode provides a smooth transition between the complementary input pairs, but is more sensitive to supply voltage variations. Keeping $\sqrt{I_P} + \sqrt{I_N}$ constant needs more elaborated circuitry and relies on the quadratic characteristics of MOSFETs, which are not strictly followed in short-channel devices. The minimum/maximum current selection provides a nearly constant g_m , but performance comes at a price – a more complicated circuit.

II. The output stage.

Rail-to-rail performance is easier to achieve at the output stage; yet, a good low-voltage output stage must meet the following requirements:

- a) a strictly controlled quiescent current
- b) a high current driving capability
- c) a simple circuit topology so that parasitic poles are avoided

OPAMP CIRCUIT(S) DESCRIPTION

Since the target supply voltage for cell design is 3 V (min 2.7V, max 3.6V), sufficient gain can be achieved with compact two-stage architectures, thus avoiding the stability problems related to multi-stage topologies. Moreover, small die area is highly desirable in modern VLSI circuits. Three compact two-stage single-supply opamps are proposed.

The first one (shown in Fig. 1) is a rail-to-rail opamp with current switching g_m control. The reference voltages for the P- and the N- current switches are provided by voltage divider M26, M18, R0 and R1, so that a smoother transition between P-and

N- stage in the middle of the CM range is achieved. Current summation is performed by a folded-cascode with floating bias-current generator.

A class AB common-source output stage was chosen with two dynamically-biased auxiliary amplifiers – M28, M34-39, M40; and M44-M50. Although slightly complicated, this output stage offers strict quiescent current control. The quiescent output current I_Q is defined by the bias current and the gain of the mirrors M37-M32 and M49-M51. The maximum source/sink current is defined by the positive feedback introduced by M37-38, M40, M35; and M45, M48, M49-50. With feedback gain α of

$$0.8, \text{ the maximum current is } I_{MAX} = \frac{I_Q}{1-\alpha} = \frac{I_Q}{1-0.8} = 5I_Q$$

Only one low-impedance node (N18/N23) is introduced in the signal path, hence the additional pole introduced is placed in frequencies far beyond the unity-gain frequency and does not affect opamp stability.

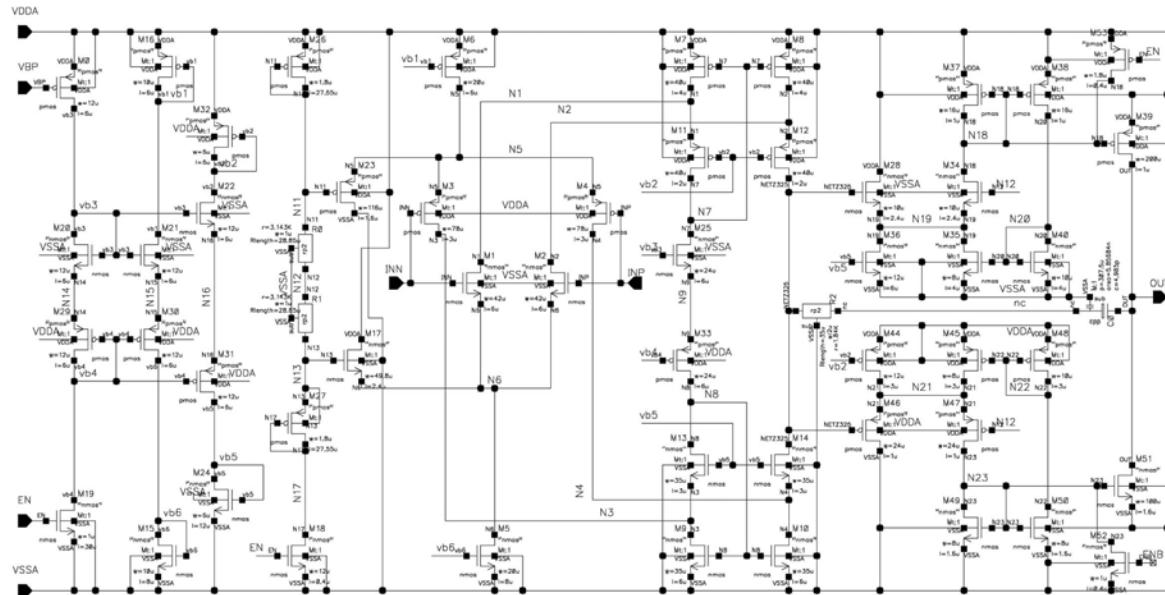


Fig. 1 R-R input opamp with current-switching g_m control

Fig. 2 shows a similar design with an “electronic zener” diode in the input stage [7] [8]. The electronic zener diode keeps the g_m constant by keeping constant the sum of the gate-source voltages of the two input stages. The reference voltage is defined by the diode-connected transistors M38 and M44. In order to achieve accurate voltage reference, the current through it must be constant. M43; M46; and M48 form a regulator that keeps the current through M43 constant. Since the W/L ratios of M38 and M43 are equal, the current through the diode-connected transistors M38 and M43 is also constant, thus keeping $V_{GS38} + V_{GS44} = \text{const}$.

Because of their robustness and excellent performance, and because the main goal was to compare the input stages, the same current summation and the same output stage are used.

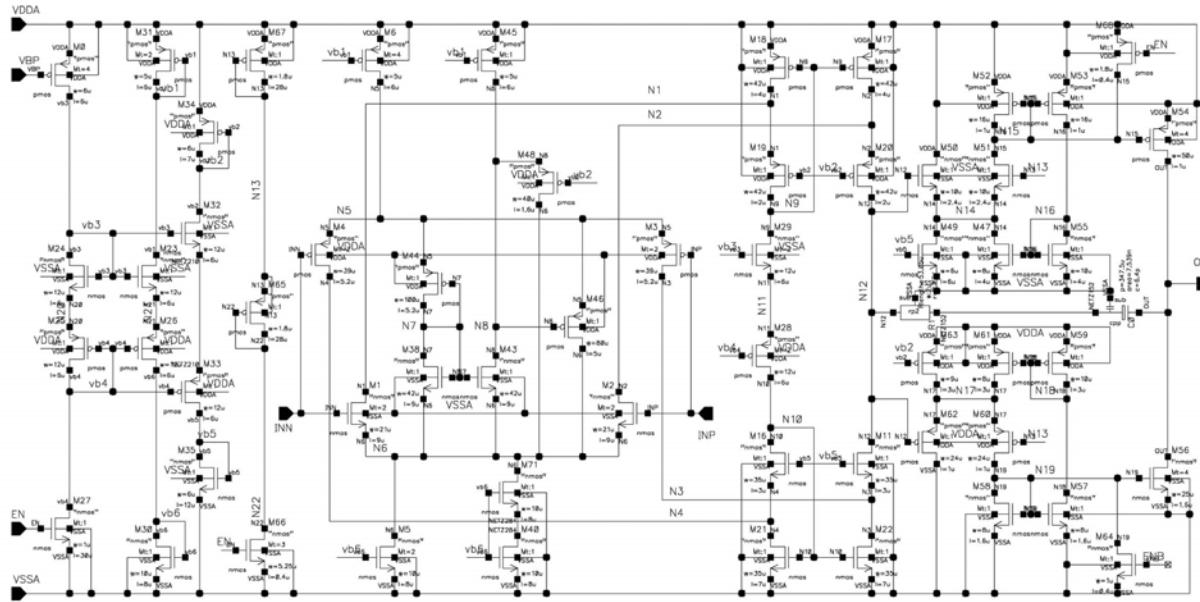


Fig. 2 R-R opamp with electronic zener diode in the gm control circuit

Fig. 3 shows a compact N-MOS input low-voltage amplifier. The input CM range is 0.9V to $V_{DD} - 0.4$ V. The output stage meets the requirements listed in the previous section: the quiescent current is defined by the bias current and equals $I_Q = 20I_B$. The maximum sink current at the output is $60I_B$. The output stage does not introduce additional poles in the frequency band of interest as the impedances at nodes N4 and N5 are low.

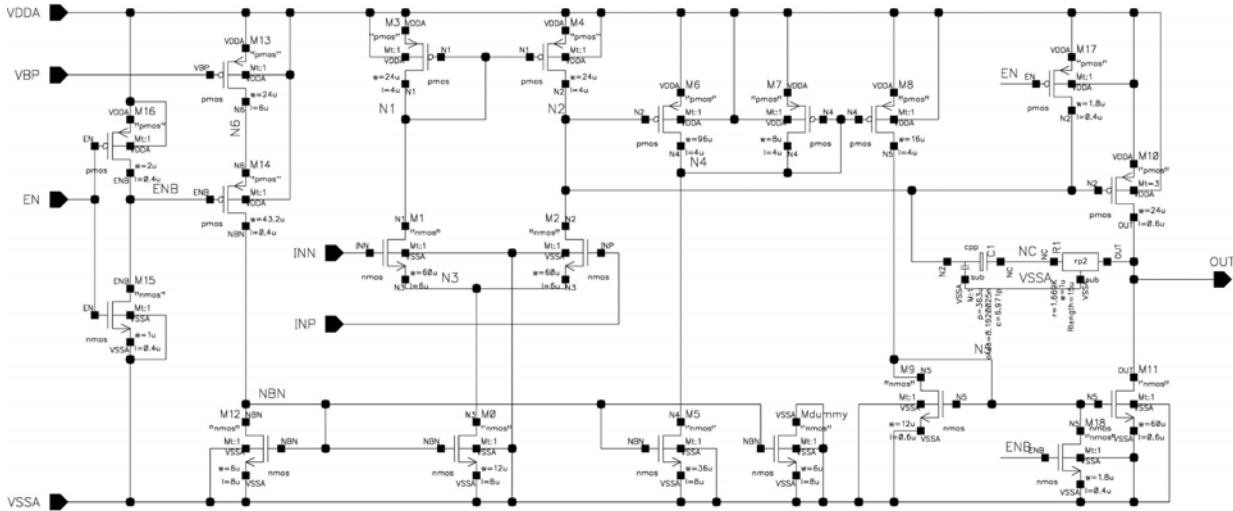


Fig. 3 Compact low-voltage two-stage opamp

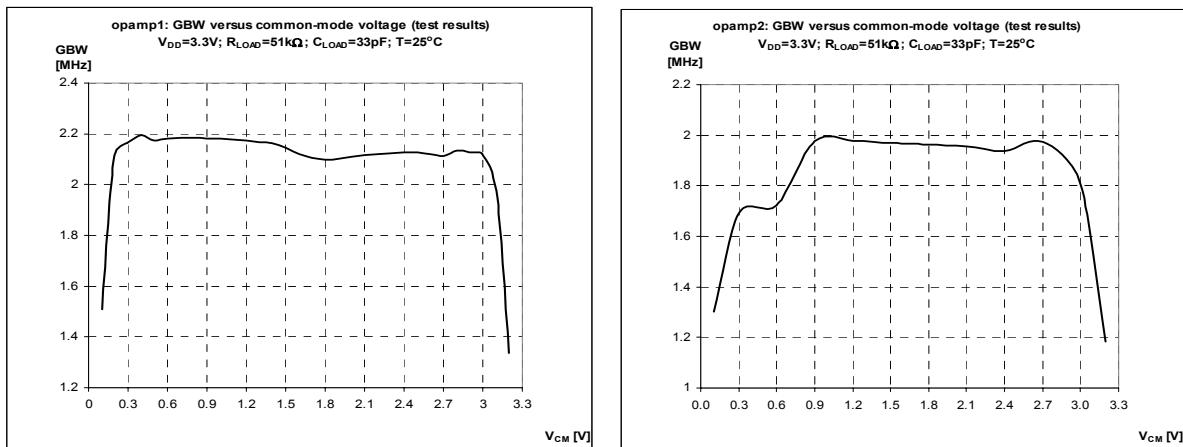
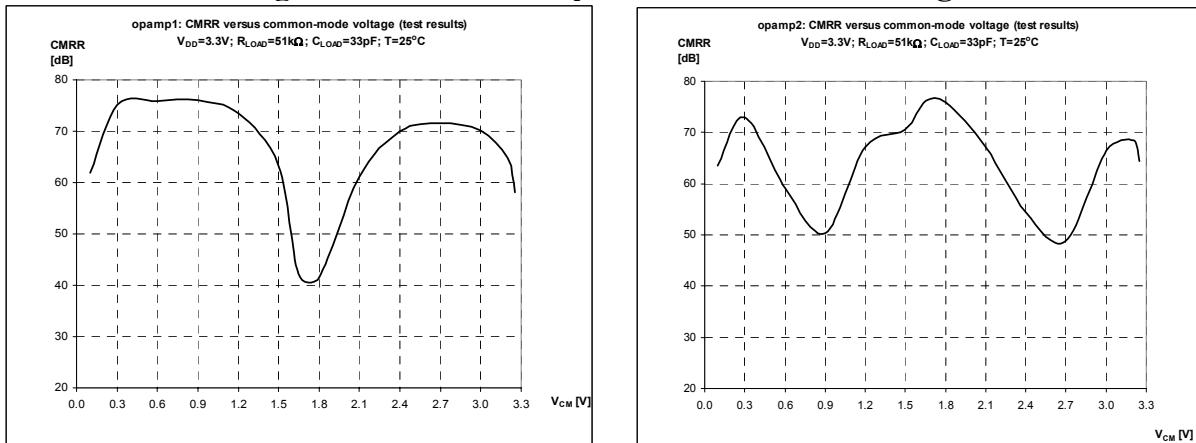
EXPERIMENTAL RESULTS

The proposed circuits are implemented in standard 0.35mm double-metal, double-poly CMOS process. Table 1 summarizes the test results of the three opamps.

Current switching offers excellent gm control – the observed deviation of gm over the CM range is less than 5%. The main disadvantage of this method is the poor CMRR – in the middle of the CM range, the P- and N-MOS pairs interchange, and hence the input offset voltage of the amplifier also changes, yielding a drop in the CMRR.

Table 1. Opamp performance summary(All parameters measured at $V_{DD}=3.3V$; $R_{LOAD}=51k\Omega$; $C_{LOAD}=47pF$; $T=25^{\circ}C$)

Parameter	Opamp1	Opamp2	Opamp3	Unit
Die Area	0.022	0.029	0.017	mm^2
Supply Voltage	2.7 – 3.6	2.7 – 3.6	2.7 – 3.6	V
Quiescent Current	296	160	320	μA
Input Voltage Range	-0.3 – $V_{DD}+0.3$	-0.4 – $V_{DD}+0.3$	0.9 – $V_{DD}-0.4$	V
Output Voltage Range	0.1 – $V_{DD}-0.1$	0.1 – $V_{DD}-0.1$	0.2 – $V_{DD}-0.15$	V
Input Offset Voltage	10	8	3	mV
Open-Loop gain	114	107	90	dB
GBW	1.99	1.96	2.67	MHz
SR (Rise / Fall)	1.97 / 1.94	2.71 / 2.57	2.08 / 2.05	V/ μs
Phase Margin	76	72	74	deg

**Fig. 4 GBW versus input common-mode voltage****Fig. 5 CMRR versus input common-mode voltage**

The electronic zener diode provides smoother transitions between the three operating regions (P-MOS pair only; both P- and N-MOS pairs; N-MOS pair only). The measured drop of the GBW for low CM voltages is due to inevitable process tolerances. The smoother transitions result in a better CMRR. Note that instead of one deep drop of CMRR, there are now two shallow drops. The summing circuit is robust and provides high open-loop gain; its main disadvantage is that the floating current source prevents operation at lower supply voltages. For supply voltages below 3V, floating current sources should be avoided.

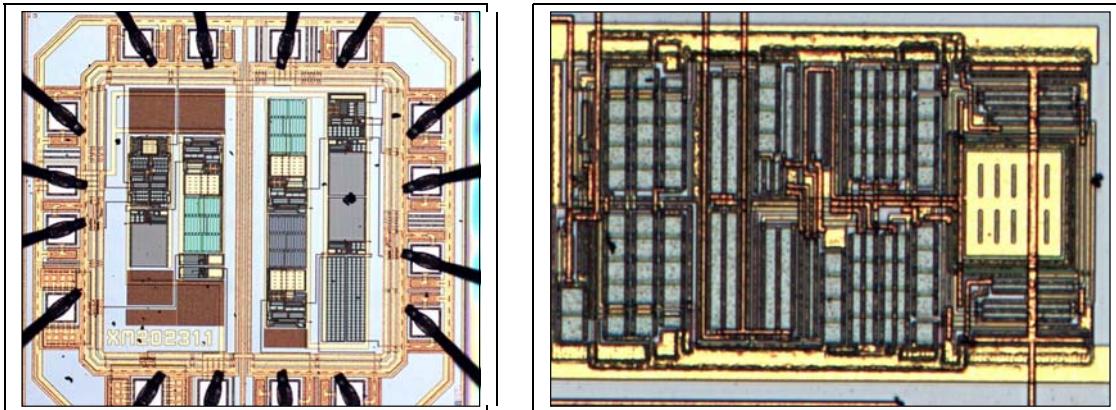


Fig. 6 Die Photograph (Opamp1 only)

CONCLUSION

Three compact low-voltage opamps have been designed in a standard “digital” 0.35mm double-metal, double-poly CMOS process. Due to their small sizes, low power consumption and low-cost fabrication process these opamps are very suitable for VLSI libraries for mixed-signal applications.

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