

ACCURATE SUPPLY CURRENT TESTING OF MIXED-SIGNAL IC USING AUTO-ZERO VOLTAGE COMPARATOR

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A novel approach to the dynamic supply current sensing based on the measurement of voltage drop across a parasitic resistance of the supply voltage metal line is presented. Then, auto-zero technique for voltage comparator offset cancellation, which provides very accurate and sensitive low voltage measurement is proposed. Therefore, we may use this as a current monitor for dynamic current testing of mixed-signal circuits without any additional element necessarily connected in series with the power supply line. The proposed current monitor was designed in a standard 0.35 μ m CMOS technology. Feasibility of this approach was investigated for a wide temperature range and process variations using Monte-Carlo analysis.

Keywords: Built-in Current Sensor, I_{DD} Testing, Auto-Zero Technique, Low Offset Comparator

1. INTRODUCTION

Recently, the supply current monitoring (I_{DD} testing) has been used to supplement the conventional logic testing for many systems that require high quality test [1]-[2]. I_{DD} testing detects an abnormally increased supply current, caused by a fault present, flowing into the device under test (DUT). In order to obtain high-speed and high-resolution I_{DD} testing, the built-in I_{DD} testing (a current monitor integrated together with the DUT) has been proposed. Most of built-in current sensors detect an abnormal current by sensing a voltage drop across a resistance element [3-7]. Figure 1 shows a principal block diagram of a common I_{DD} sensor arrangement. In this structure, the supply current is transformed to voltage using the resistive sensing element. This voltage is then compared with an external reference voltage by a voltage comparator. The resistive element is usually implemented as a MOS transistor or a combination of a MOS transistor and a diode. In order to obtain high sensitivity to the abnormal defective current, the sensing element must have a high resistance that, on the other hand, causes undesired degradation of the DUT supply voltage.

Thus, for low voltage circuits, is very important that the supply voltage degradation caused by the current sensor is minimized. Therefore, a piece of metal wire, connecting the supply pad with the DUT core, is used as the resistive element in some current monitors [2-4]. This topology achieves a rather small voltage drop across the sensing element (in order of few mV). Thus, a simple voltage comparator cannot be used as the evaluating circuit (Fig. 1) due to its high input voltage offset (in order of tens mV) of the input differential pair in a CMOS technology.

Therefore, auto-zero stabilization is utilized in the current monitor proposed in this paper as a smart and efficient solution for reduction of the voltage comparator input offset. It also helps to compensate any other ineligible effects such as the offset drift (caused by temperature variations, ageing, power supply deviations, mechanical stress, etc.), and provides the current sensing with high accuracy. Some other advantages of auto-zero structure include the possibility to feature a high

open loop gain and a high power supply rejection ratio. CMOS technology is suitable for implementation of such a design, due to its analog switch capabilities and low power feature.

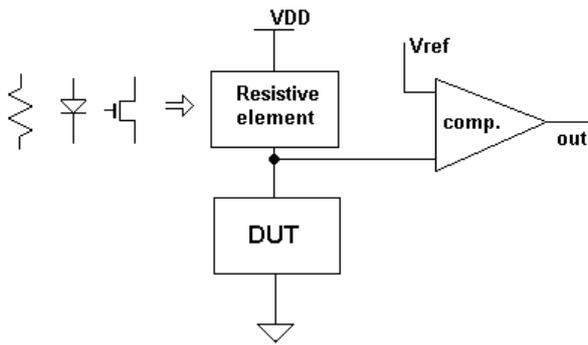


Fig.1. Usual topology of a built-in current sensor

voltage comparator, which compares the supply current value measured on a parasitic resistance of VDD line to the reference voltage. This approach offers very accurate and sensitive measurement of small currents. The proposed circuit has been designed in a standard 0.35 μ m CMOS technology.

During last couple of years, we have worked on different approaches to on-chip current testing. The more complex design, proposed in [8], describes the current conveyor architecture, which is used to convey the supply current into a threshold detector distinguishing whether the current value is nominal or defective. Furthermore, an off-chip supply current sensing and evaluating method for analog circuits using artificial neural networks was proposed in [9].

In this paper, we propose a simple supply current sensor using an auto-zero compensated

2. DESIGN OF THE CURRENT SENSOR

The main task of any current-based test method is sensing the current, which is drawn by the DUT using a sensing element with a minimal resistance in order to reduce the undesired power supply degradation. Therefore, we use a certain small parasitic resistance of a metal layer used in every chip to connect the supply voltage pad to the circuit core as shown in Figure 2. This solution has no substantial influence on the DUT performance since there is no considerable voltage drop across the current sensor.

To achieve low resistance of the sensing resistor the highest layer of metallization with the smallest sheet resistance is used. Since the AMS 0.35 μ m CMOS process, used to design the sensor, is three metal layer technology, we employed the third metal layer (with sheet resistance of 50m Ω / \square) to implement the sensing resistor. Thus, if we consider an acceptable serial resistance of 1 Ω to sense the current, this implies the metal line of twenty squares.

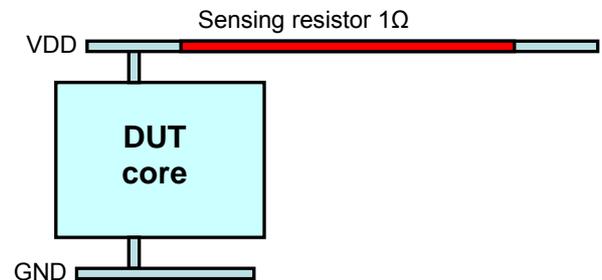


Fig.2. Sensing element

There is a very small voltage drop V_{do} created by small supply currents from the range of hundreds of μ A to tenths of mA across this small serial resistance. In a standard CMOS technology, there is a problem to guarantee low input offset voltage in operational amplifiers. Additionally, both the offset magnitude and its polarity are unpredictable. Since the magnitude of input voltage offset in CMOS technology may achieve hundreds of mV, it is necessary to use an offset compensation technique to reduce the input offset, especially in high accuracy applications.

Generally, there are more effects influencing the amplifier behavior closed to DC area:

- Input offset voltage – mainly due to the process variations and lithographic errors
- Offset drift – due to temperature changes, ageing, and mechanical stress (time varying offset)
- Flicker (1/f) noise – varies inversely with transistor area

In our work, we use the auto-zero technique as a dynamic approach to input offset cancellation [10]. The main advantage of the selected approach is that this technique reduces also the flicker noise and the offset drift. Therefore, the proposed solution is designated for very sensitive current measurement with high accuracy.

2.1 Auto-Zero Technique

The simple auto-zero topology is shown in Figure 3, where the voltage comparator has its input offset voltage V_{os} . The signs plus and minus inside the voltage offset symbol mean that we do not consider a particular offset polarity.

If the switches Φ_1 are turned on, then the comparator is in unity-gain negative feedback loop configuration. This mode is called the offset cancellation phase. Then, the output voltage is expressed by the following equation:

$$V_{out} = -\frac{A_v}{A_v + 1} V_{os} \cong -V_{os} \quad (1)$$

Thus, the offset voltage V_{os} is stored in capacitor C_1 with the opposite polarity, and in the next phase, when switches Φ_1 are turned off and switches Φ_2 are turned on, this voltage is in series with the regular offset voltage at the amplifier input and they compensate each other. Problem with this simple topology is that the switch Φ_2 at the comparator input is affecting the current signal sensed. Thus, the output signal might exhibit false comparison results while the input switch Φ_2 is kept turned off. Therefore, we insert additional switch Φ_2 , and capacitance C_2 at the output of comparator. Consequently, when the switches Φ_2 at the input are turned off, then the comparator output is disconnected by the output switch Φ_2 , controlled by the same clock, and the previous state of the output is stored on the capacitance C_2 . An output buffer for minimal loading of this switch and capacitance C_2 is embedded in the circuitry. A simple inverter stage has been used as the buffer since there are only two states of the output signal. If the current flowing through the serial resistor R_s produces a voltage drop V_{do} higher than the reference voltage V_{ref} , then the output is in its high state. This indicates an elevated current value representing a defective DUT. Low state of the output represents a normal supply current expected in the fault-free state of the DUT.

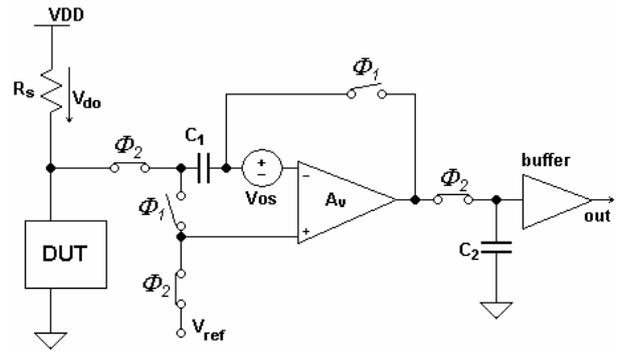


Fig.3. Current sensor, block diagram

2.2 Non-overlapping clock

Switches Φ_1 and Φ_2 , realized by NMOS transistors are controlled by two clock signals. There is a special timing requirement for these two clock signals due to the fact that the switches Φ_1 and Φ_2 are not supposed to be turned on simultaneously. Therefore, we designed a simple circuit to generate two non-overlapping clocks, as depicted in Figure 4. Specific design of the inverters allows realization of the clock signals using only minimum circuit components.

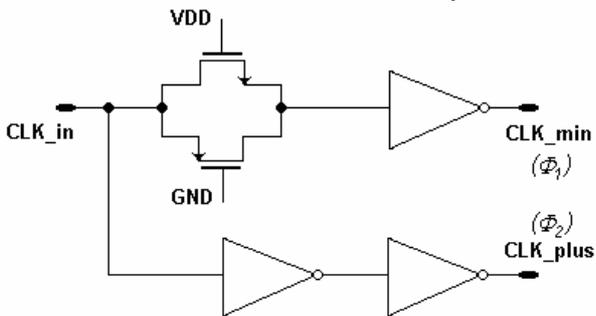


Fig.4. Non-overlapping clock

Specific transistor sizing shifts the threshold voltages of all the inverters in lines CLK_min and

CLK_plus from the usual value of $V_{DD}/2$ to desired values providing the required timing. There are two outputs of the proposed non-overlapping clock generator: CLK_min, which controls the switches Φ_1 , and CLK_plus, controlling the switches Φ_2 . Signal CLK_in has a duty cycle 90% because the offset cancellation phase (switches Φ_1 turned on and Φ_2 turned off) is supposed to be rather shorter (due to a shorter time needed to compensate the offset voltage) than the normal phase, when the input signal is directly sensed, compared, evaluated, and sent to the output.

2.3 Rail-to-rail Comparator

Since the voltage drop V_{do} across the current sensor is very small, the reference voltage V_{ref} , connected to the non-inverting input of the voltage comparator, is near to the supply voltage V_{DD} . For further considerations we determine usage of a comparator with rail-to-rail input. This solution has also another advantage: such a current monitor might be inserted also in a metal line connecting the ground to the DUT, with minor changes needed in the design. The only modification would be the value of V_{ref} selected near to the GND. In some test applications we may use two current sensors - one connected in V_{DD} line and the other in GND line. Therefore, if the monitor placed in V_{DD} line indicates a defect in DUT and monitor placed in GND line signals good DUT, we know that there is a leakage current somewhere in the circuit.

The designed rail-to-rail voltage comparator is shown in Figure 5. It is one-stage circuitry with two differential amplifiers involved, the first one composed by NMOS transistor pair M_{13} and M_{14} , and the second one consisting of PMOS transistors M_{15} and M_{16} . The current source i_{bias} is set to the value of $4\mu A$ for biasing the current sources M_3 and M_4 of the respective differential stage.

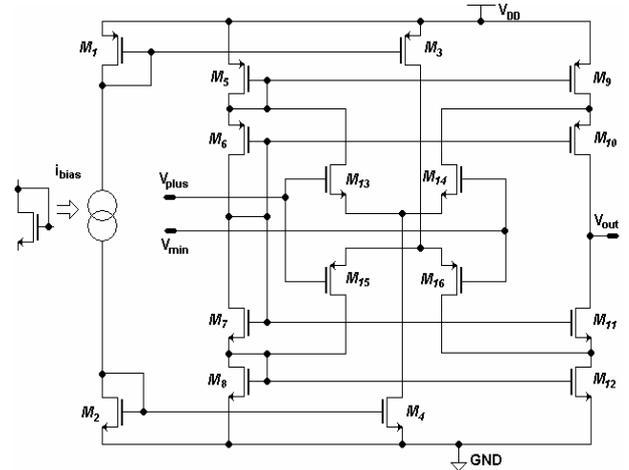


Fig.5. Rail-to-rail comparator

3. SIMULATION RESULTS

The feasibility of the approach and the main properties of the proposed current sensor were verified by simulations done in Cadence environment using AMS 0.35 μm CMOS technology with supply voltage of 3.3 V. The achieved results show that the most important feature, affecting the monitor performance significantly, is the sensing resistor R_S as its particular resistance value determines the operating range, in which the sensor gives the accurate current monitoring. Thus, the accuracy of the proposed current sensor in a particular working range is given by the input offset cancellation ability of the auto-zero based voltage comparator. Table 1 demonstrates the accurate operating ranges determined by the respective R_S value.

Table 1 Accurate working ranges of the current sensor

R_S [Ω]	Working range (I_{DD})	V_{domax} [mV]	Accuracy (worst case)
2	50 μA ÷100 μA	0.2	10%
1	100 μA ÷1mA	1	5%
1	1mA÷10mA	10	0.5%
0.1	10mA÷100mA	10	0.05%

Selection of the proper working range is a compromise between the accuracy and the maximum voltage drop allowed across the current sensor. Typical simulated offset of the comparator was $1\mu\text{V}$, and the worst case offset result obtained by Monte-Carlo analysis was $5.2\mu\text{V}$ even for high temperatures. Very high accuracy given by low offset is achieved for the current range from 10 mA to 100 mA. However, these results represent theoretical accuracy obtained only from simulations with the ideal reference voltage V_{ref} , which does not vary with temperature and the supply voltage fluctuations.

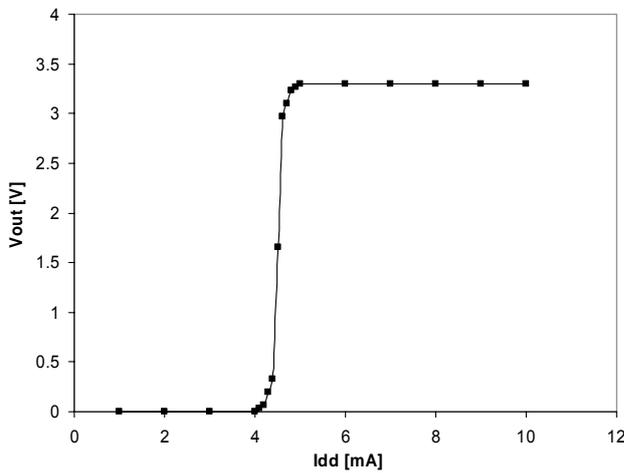


Fig.6. Output of the proposed current sensor

The output signal of the monitor is shown in Figure 6. The reference voltage was set to 4mV, the value of the parasitic serial resistance was 1Ω . Low level of the output signal represents good state of the tested circuit while its high level indicates defective circumstance.

Dynamic behavior of the proposed current sensor is shown in Figure 7. There are two curves, the bottom curve displays the voltage drop on the resistive element, and the upper waveform the current sensor output. Time needed to transfer a fault appearance from the resistive element to the buffer output is approximately $0.4\mu\text{s}$ and it is so called reaction time. Time for recovery of the output from fault state to normal working state is the recovery time and its simulated value is $4.4\mu\text{s}$. These two

dynamic parameters play a dominant role in determining the maximum testing frequency.

In analog integrated circuits, the supply current consumption is usually not negligible as it is in their digital counterparts. Therefore, an on-chip current monitor used for analog circuit testing should handle high currents and a wide range of supply currents. Since most of the known current sensors invoke unacceptable DUT performance degradation due to a significant voltage drop across the monitor itself, they are generally impractical for real test applications. The principle, proposed in this paper, minimizes the undesired voltage drop across the current sensor (even for very high supply currents to be measured) to the value commonly observed and caused by the parasitic serial resistance of the metal lines used. Thus, a slightly modified built-in current sensor can offer a wide range of possibilities and features useful for current testing of analog and mixed-signal circuits.

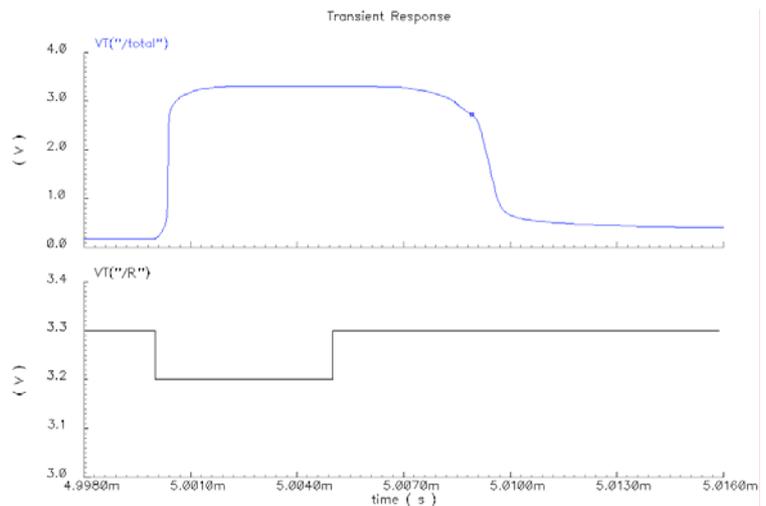


Fig.7. Dynamic behavior of the proposed current sensor

4. CONCLUSION

A new on-chip dynamic current sensor for accurate measurement of the dynamic supply current in a wide current range is proposed. By employing the parasitic resistance of the metal line of VDD routing as a sensing element, the proposed current sensor does not cause additional undesired DUT supply voltage degradation. It is able to measure dynamic currents in the range from 50 μ A to 100mA without affecting the DUT performance. The proposed current monitor can be used to sense current flowing through V_{DD} or GND metal connection because of a rail-to-rail voltage comparator being used. There is one-bit information generated at the sensor output indicating the actual state of the DUT, either good or defective. The developed monitor is dedicated primarily to testing of large mixed-signal circuits. Thus, the reference voltage V_{ref} necessary for the comparator threshold might be generated by a voltage reference circuitry usually present in the analog part of the whole tested design. On the other hand, the clock signal CLK_{in} for auto-zero based input offset cancellation circuit could be acquired from a digital part of the mixed DUT design. Modifying the current sensor in this way might simplify the sensor design essentially, where no extra input pins or on-chip circuitry providing those signals would be needed.

Current consumption of the whole current sensor is 23 μ A. The proposed sensing circuit is implemented in AMS 0.35 μ m CMOS technology and will be fabricated together with experimental analog and digital circuits in the near future.

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