THE INFLUENCE OF GEOMETRY AND TEMPERATURE ON THE PARAMETERS OF INTEGRATED CAPACITORS

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The research in this paper is focused on poly-poly capacitors, whose electrodes are built of polysilicon with insulation layer (SiO_2) between them. Different models are used for characterization - cpolybr3, cpoly and cpolyrf. Some of them present the capacitor as a three terminal device (cpolybr3, cpolyrf). The simulations are done in the CADANCE environment with Spectre Circuit Simulator. Different connections are made to explore the influence of the layout over the basic characteristics of the capacitor, depending on the number of stripes (parts the capacitor is split into). The value of the explored integrated capacitors is 0.1÷5pF. Two technologies are used – AMS 0.35 um SiGe BiCMOS and 0.8 um SiGe BiCMOS.

1. INTRODUCTION

Capacitors are a class of passive elements useful for AC coupling and constructing timing and phase shift networks. They are relatively large devices and store energy in electrostatic fields. The microscopic dimensions of integrated circuits preclude the fabrication of more than a few hundred Pico farads of capacitance. Even this tiny amount is sufficient for certain applications. Most analog integrated circuits contain at least one capacitor.

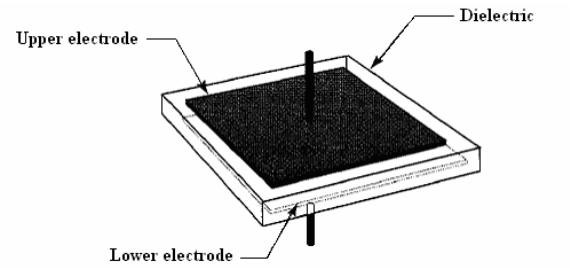

Fig. 1. Parallel-plate capacitor structure

All capacitors used in integrated circuits are parallel-plate capacitors. They consist of two conductive plates called electrodes and insulating material between them called dielectric (Fig. 1). The value of the parallel-plate capacitor can be calculated using following equation:

$$C = 0.0885 \frac{Ae_r}{t} \quad , \tag{1}$$

where C is the capacitance in picofarads (pF), A is the area of either electrode in square microns (μm^2), t is the thickness of the dielectric in Angstroms (Å), and e_r is a dimensionless constant called the dielectric constant.

Reducing the thickness of the dielectric increases its capacitance, but it also increases the electric field imposed across it. That is why it is so difficult to integrate capacitors of more then a few hundred picofarads.

The poly-poly integrated capacitors consist of two polysilicon layers with insulation layer of SiO_2 between them. Both of the electrodes consist of existing depositions, but the capacitor dielectric is unique to this structure and requires a process extension. The simplest way to form this dielectric is to eliminate the interlevel oxide (ILO) deposition that normally separates the two polysilicon layers, and in its place substitute a thin oxide grown on the lower polysilicon electrode. Using this technique, a capacitor forms wherever the two poly layers lay on top of one another.

The voltage modulation of poly-poly capacitors is relatively small, as long as both electrodes are heavily doped. The typical value of voltage modulation is 150 ppm/V. The temperature coefficient of a poly-poly capacitor also depends on voltage modulation effects and is typically less then 250 ppm/^{o}C.

It is important to mention that the two plates of a poly-poly capacitor are not wholly interchangeable. The upper electrode usually has less parasitic capacitance than the lower electrode.

The capacitors can be characterized with temperature coefficient of a capacitor (TCC). The TCC is given by

$$TCC = \frac{1}{C}\frac{dC}{dT}, \tag{2}$$

A typical value of TCC for a poly-poly capacitor is 20 ppm/^{o}C.

2. SIMULATION RESULTS OF THE INTEGRATED CAPACITORS ANALYSES

2.1. Layout influence

The layout influence over the basic characteristics of the integrated capacitors is studied in CADENCE for the capacitors with cpolybr3 model. It is analyzed for AMS 0.8 um SiGe BiCMOS technology. The layout of capacitor built of two stripes is shown at Fig. 2. Its symbol has three pins. Fig. 3 shows the Pi equivalent circuit, which includes several parasitics: Rp1, Rp2, Csub and Rsub. Rp1 and Rp2 are the resistances for the poly1 and poly2 materials. Csub is parasitic capacitance, which depends on the ratio between poly-poly oxide and poly1-substrate oxide. And Rsub is the substrate resistance.

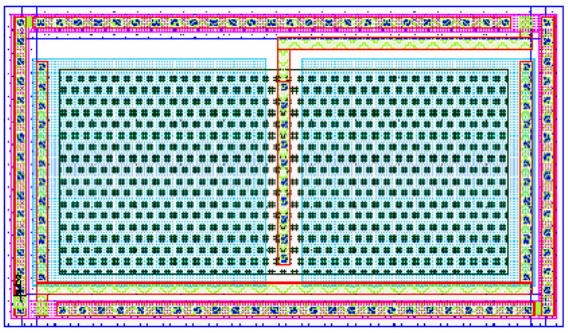

Fig. 2. Layout of a capacitor cpolybr3

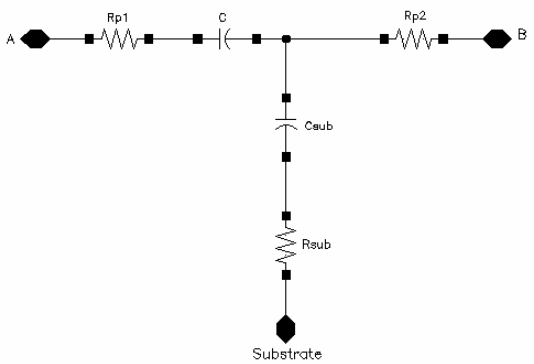

Fig. 3. Pi equivalent circuit of a capacitor

Cpolybr3 can be placed on two different kinds of layers: P-substrate or N-well. P-substrate is used whenever the capacitor is a casual one and its influence on the designs performance is not crucial. If the cpolybr3 is used on top of P-substrate, then the substrate pin should be connected to ground. If the cpolybr3 is used on top of N-well, then the substrate pin should be connected to the voltage supply.

Different setups were employed for investigation of all the capacitors properties. Throughout the simulations the number of capacitor stripes was changed in ratio 1:3:10.

Fig. 4 shows the circuit utilized for simulation of: the capacitor, when it is used as a low-pass filter and placed on top of P-substrate. Reverse positioning is used. Simulations are made in the frequency range from 1 to 1THz. Some of the results are shown in Fig. 5.

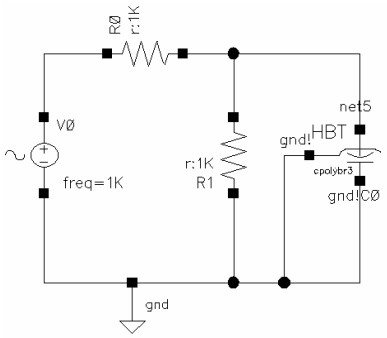

Fig. 4. Analysis of capacitor placed on top of P-substrate

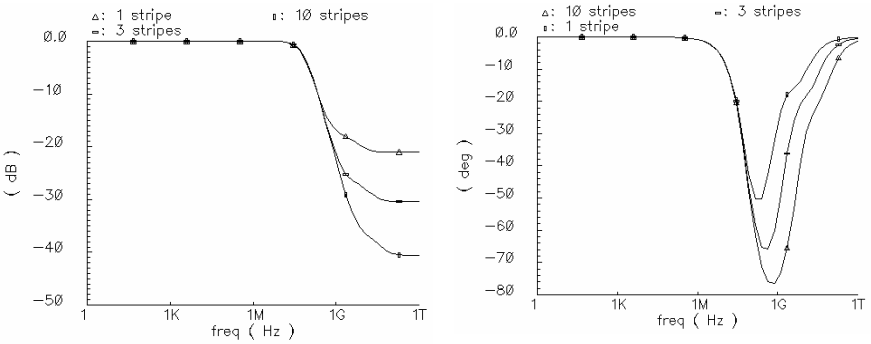

Fig. 5. Simulation results for AC magnitude and phase

The difference in the waveforms for AC magnitude and AC phase can be explained if the capacitor parasitics are taken into account. A summary of all those parasitics and dimensions for 4pF capacitance are shown in Table 1.

Table 1

Capacitance: 4pF	**1 stripe**	**3 stripes**	**10 stripes**
Area	$2.23*10^{-9}$	$7.4*10^{-10}$	$2.21*10^{-10}$
Perimeter	189um	109um	59um
Csub	152fF	50fF	15fF
Rsub	100?	100?	100?
Rp1	9.33?	9.33?	9.33?
Rp2	26.7?	26.7?	26.7?

It is evident that the more stripes the capacitor has the smaller parasitic capacitance is. In other word it becomes closer to the ideal capacitor.

The same circuit is used for studying the capacitor cpolybr3 placed on top of N-well. The capacitor is used as a low-pass filter once again, but the substrate pin is connected to the voltage supply (Fig. 6). Fig. 7 shows the simulation results for AC magnitude and phase.

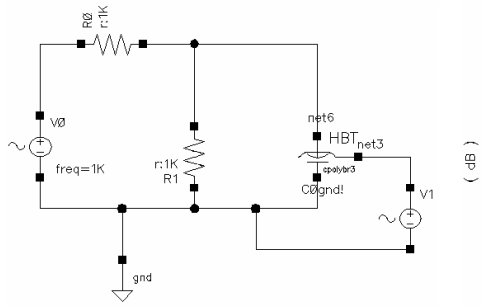

Fig. 6. Analysis of capacitor placed on top of N-well

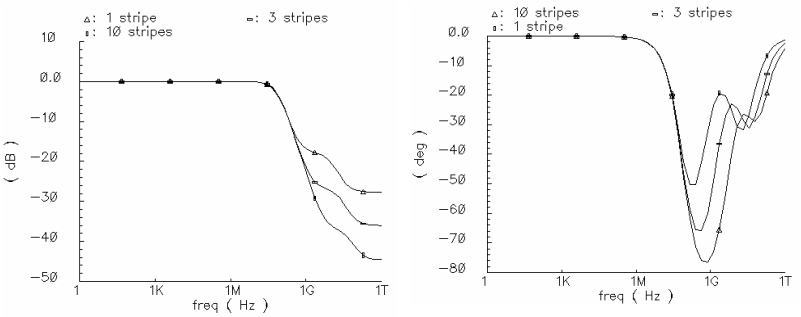

Fig. 7. Simulation results for AC magnitude and phase

Fig. 8 shows the capacitor used as a high-pas filter, placed on top of P-substrate. Proper positioning is used. The results from AC analyze in the frequency range up to 1 THz, depending on the number of stripes – parts the capacitor is split into, are shown in Fig. 9.

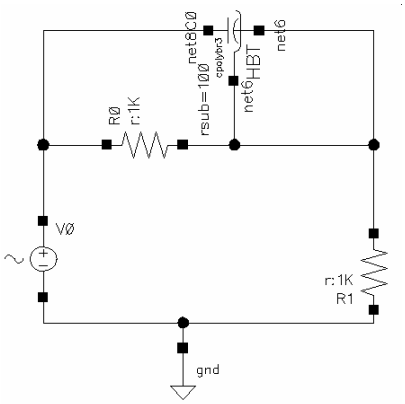

Fig. 8. Analysis of capacitor placed on top of P-substrate

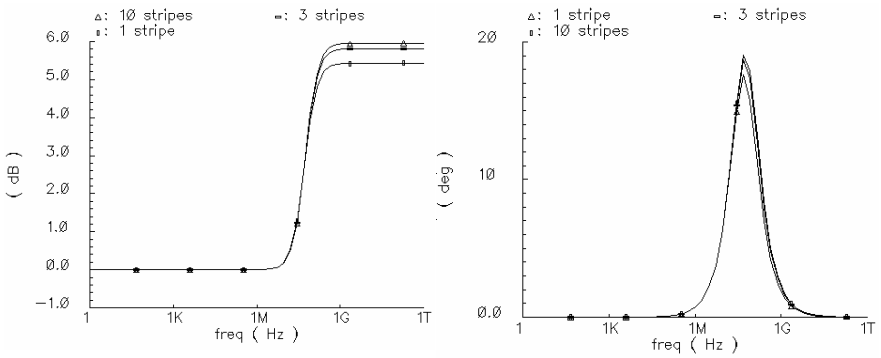

Fig. 9. Simulation results for AC magnitude and AC phase

The circuit shown in Fig. 10 is used for examination of the capacitor cpolybr3 as a high-pass filter. The capacitor is placed on top of N-well so the substrate pin is connected to the power supply. The AC analyses are made and the simulation results for AC magnitude and phase are shown in Fig. 11.

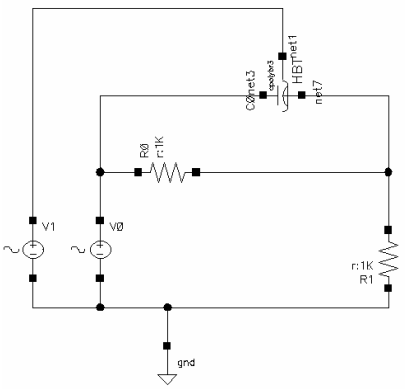

Fig. 10. Analysis of capacitor placed on top of N-well

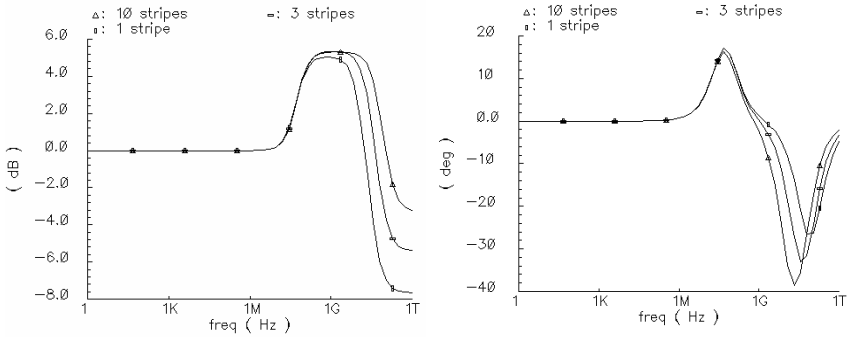

Fig. 11. Simulation results for AC magnitude and AC phase

2.2. The real capacitor parasitics

In order to examine the real capacitor a simple layout is created using Virtuoso Layout Editor program. For this example a 2pF capacitor with two stripes and w/l ratio 1:1 is used. A comparison is made between the three deferent capacitors – capacitor placed in P-substrate, capacitor placed in N-well and the layout of a capacitor placed in P-substrate with parasitics (extracted view of the capacitor). Results from the analysis are shown in Fig. 12.

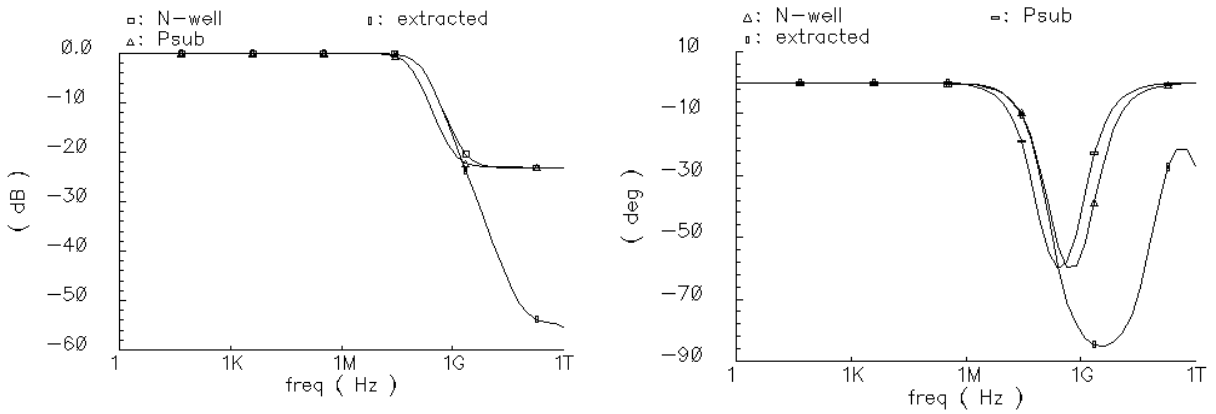

Fig. 12. Comparison results

From these waveforms can be seen that the extracted capacitor approximates the ideal capacitor characteristics.

2.3. Temperature influence

The capacitor models cpoly and cpolyrf are used to study the temperature influence over the basic parameters of integrated capacitors. They are designed for y AMS 0.35 um SiGe BiCMOS technolog. Typically, contacts are placed over the whole upper plate of cpolyrf capacitor, and the lower plate contacts are located around the three sides of the capacitor. The REF pin of the capacitor always has to be connected to ground.

The simulations for cpolyrf and cpoly are done in CADENCE using the circuit shown at Fig. 13 and Fig. 15. The selected temperature range is -50÷+150°C. Fig. 14 and Fig. 16 give the temperature dependence of the capacitance value.

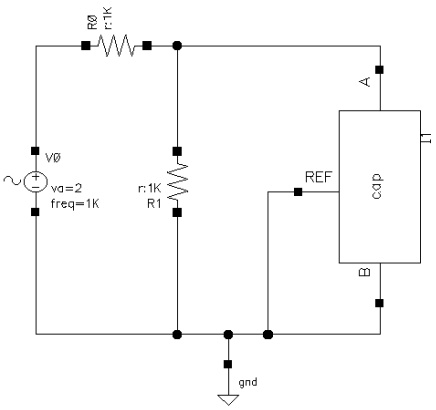

Fig. 13. Schematic setup for the capacitor cpolyrf

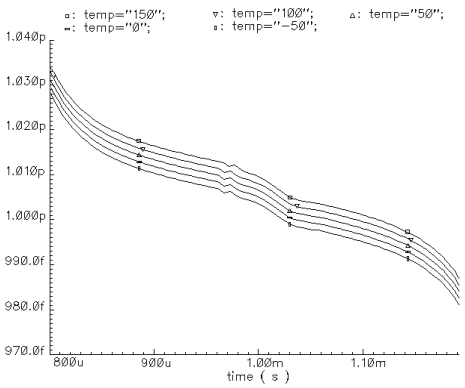

Fig. 14. Temperature influence over the capacitance variation for cpolyrf

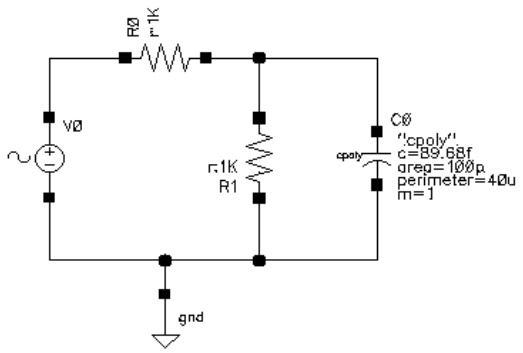

Fig. 15. Schematic setup for the capacitor cpoly

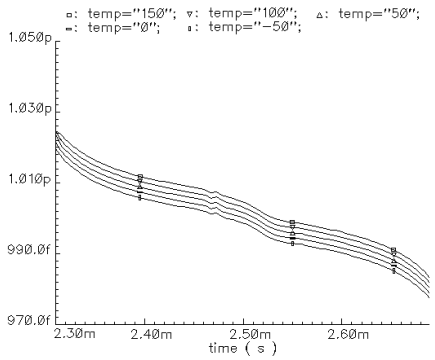

Fig. 16. Temperature influence over the capacitance variation for cpoly

3. CONCLUSION

Capacitance is not as easily integrated as resistance. Without using exotic materials such as titanates, only a few hundred picofarads of capacitance can be integrated on a single die. Even this relatively small amount of capacitance is satisfying for many applications, including timers, capacitive dividers, and active filters.

Based on the simulation results for capacitor cpolybr3, designed for AMS 0.8 um SiGe BiCMOS technology, the following conclusions can be made:

- The difference in the waveforms for cpolybr3, designed for AMS 0.8 um SiGe BiCMOS technology, can be explained if the capacitor parasitics are taken into account. A summary of all those parasitics and dimensions are shown in Table 1.
- It is obvious that the more stripes the capacitor has the smaller the parasitic capacitance is. The more stripes are used in the capacitor the more capacitor behaves as an ideal one. That is because the capacitance to the substrate is smaller.
- Capacitors placed on top of N-well are good for use in special places because they provide a better barrier for the currents flowing to the substrate.

On the basis of results for capacitors cpoly and cpolyrf, designed for AMS 0.35 um SiGe BiCMOS technology can be said that temperature influence of the capacitance is relatively small. When the temperature is changed from -50 to +150°C, the capacitance vary from 5fF up to 10fF.

4. REFERENCES

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