Chart Oriented CAD Tool for CMOS Transistor Sizing

Danica Stefanovic*/**,
Marc Pastre*, Maher Kayal*, Vanco B. Litovski**
* Swiss Federal Institute of Technology, Electronics Labs, STI/IMM/LEG,
CH-1015 Lausanne Switzerland.
** Faculty of Electronic Engineering, University of Nis, Beogradska 14, 18 000 Nis, Yugoslavia.
danica.stefanovic@epfl.ch, marc.pastre@epfl.ch, maher.kayal@epfl.ch, vanco@elfak.ni.ac.yu

This paper presents a new chart-based approach for MOS transistor and elementary analog building blocks (such as differential pairs, current mirrors, cascode stages, etc.) sizing. A standalone PC-windows based tool has been developed. This tool is dedicated to the resolution of a complete set of equations based on EKV MOS model [3,4] of the transistor over its whole operating range. It takes into account the circuit topology as well as user's defined constraints. A design methodology will be presented to enable optimum design choices over full range of inversion level (weak, moderate or strong) of MOS transistor. The implementation of charts aimed at reducing the efforts in determining DC bias point, small signal parameters, noise, layout area and several other analog design parameters will be described.

1. INTRODUCTION

Analog design depends heavily upon designers' expertise and knowledge. The design procedure can be very complex, but the goal is always the same – discover the tradeoffs and find the optimal solution [1,2].

Many computer-based tools are made to help in the design tasks, a lot of them fail to fully exploit real human skill being too automatic. In order to explore essential aspects of design, the designer uses a simulator as a tool which allows to change the value of the circuit parameter and to observe the effect. But, in this way the discovery of a tradeoff between two performances can be very long and difficult.

Using the simulator as unique tool to accomplish analog circuit design is very limitative due to its global simulation approach (AC, DC, transient, etc.). Sometimes a very large number of simulations are mandatory to reach certain tradeoffs at circuit level such as gain bandwidth, noise, linearity, etc.

Also, analog circuit design is often performed by circuit partitioning into basic analog structures. Discovering all features concerning the basic analog structures behavior can help to easily determine the features of an analog circuit and to discover important tradeoffs.

The proposed chart oriented CAD tool is entirely dedicated to design of basic analog structures in order to enable optimum design choices and to reduce efforts in determining DC bias point, small signal parameters, speed, noise, mismatch, layout area and several other analog design parameters. A transistor level calculator is

capable of exploring some complex relations and the charts display performances interactively.In this way, the tool shows all dependencies and characteristics of analog structures at one glance and allows every design task to be carried out very easily. The simulator is used only for fine tuning and the number of simulation runs is reduced to minimum.

2. PARAMETERS SET

Usually, analog designer is faced to one very common task that consists of setting the geometrical dimensions (width/length) and bias current of each transistor of a circuit. On the one side there is a set of circuit level parameters, such as gain, speed, noise, linearity, dynamic, consumption, layout area, etc, and on the other side there is a set of transistor level parameters, such as saturation voltage, small signal parameters, equivalent noise, etc.

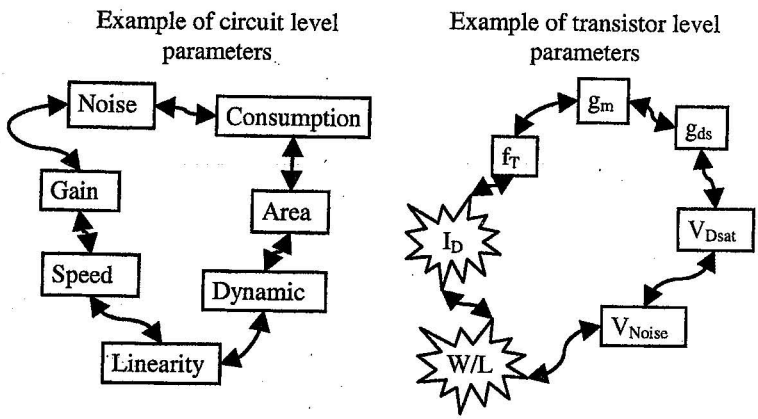

Figure 1. Circuits and transistor parameters

Every transistor parameter has to be determined to achieve optimal or specified circuit parameters. But, the interdependence between circuit and transistor level parameters is very strong. In order to find the design tradeoffs, the designer's knowledge is mandatory to drive a set of equations describing the circuit level specifications as well as transistor level parameters.

The proposed chart approach uses a complete set of equations based on EKV MOS model [3,4] of the transistor over its whole operating range. The transcription of this set of mathematical relations into an appropriate interactive graphical representation is implemented. This methodology was selected in order to give the designer an intuitive or "physical" understanding of the device behaviour.

The user-friendly graphic interface [5] allows analog designer to enter different input parameter sets, to change the basic parameters and to observe at the same time the dependencies and the changes of all other parameters. The designer doesn't have

the impression that he works with the set of equations, he is concentrated on an analog basic structure design and its important features and dependencies. This important property can also be used very efficiently in educational purposes, because all basic analog blocks can be presented in a very simple and intuitive way.

3. MOS TRANSISTOR SIZING USING EKV MODEL

The most elementary analog block is a transistor cell (NMOS or PMOS). The important parameters and equations (derived from EKV MOST model [3,4]) of one simple transistor for hand calculation are summarized and shown in Table I. The EKV MOS model is based on the description of the normalized g_m/I_D characteristic which links weak to strong inversion in a continuous way. This is very suitable for analog circuit design having transistors working in strong, moderate and weak inversion [6]. To describe the inversion level, the inversion factor I_F is defined as:

$$I_F = \frac{I_D}{2n\mu C_{ox}\frac{W}{L}U_T^2} = \frac{I_D}{2nK_p\frac{W}{L}U_T^2} \qquad (1)$$

		strong inversion	weak inversion
DC params.	I_D, U_D, U_S, U_G	$saturation: I_D \approx \frac{\beta}{2n}(U_G - U_{TO} - nU_S)^2$ $triode: I_D \approx \beta\left(U_G - U_{TO} - \frac{n}{2}(U_S + U_D)\right)(U_D - U_S)$	$saturation: I_D = I_{DO}e^{\frac{U_G - nU_S}{nU_T}}$ $triode: I_D = I_{DO}e^{\frac{U_G}{nU_T}}\left(e^{\frac{U_S}{U_T}} - e^{\frac{U_D}{U_T}}\right)$
	U_{dsat}	$\frac{U_G - U_{TO}}{n}$	$\approx 4U_T \approx 100mV$
small signal params	g_m	$\sqrt{\frac{2\beta I_D}{n}}$	$\frac{I_D}{nU_T}$
	g_{ds}	$g_{ds} = \frac{I_{Dq}}{U_A}$, $U_A = f(L)$, L↑→Gain↑	
	g_{ms}	$n \cdot g_m$	
speed	capac	C_{gs}, C_{gd}, C_{gb}, C_{sb}, C_{db}, C_{gsov}, C_{gdov}, C_{gbov}	
	f_t	$\frac{g_m}{2\pi C_{gs}}$	
Vsr noise	thermal	$f(\frac{1}{g_m})$	
	flicker	$f(\frac{1}{W \cdot L})$	
layout	area	$f(W \cdot L)$	

Table I EKV MOS model for hand calculation

Where I_D is the drain current, n the body factor, W/L are geometrical parameters of MOS transistor and the U_T is thermodynamical voltage [3,4]. With:

- $I_F > 10$: the transistor is in strong inversion,
- $0.1 < I_F < 10$: the transistor is in moderate inversion
- $I_F < 0.1$: the transistor is in weak inversion

An important design point is the choice of the gm/I_D ratio as a measure of the translation of current into transconductance [7] (gm efficiency and consumption efficiency). At the same time, it gives an indication of the device operating region (strong, moderate or weak). For circuit design this means: the greater the gm/I_D value, the greater the transconductance at a constant current value.

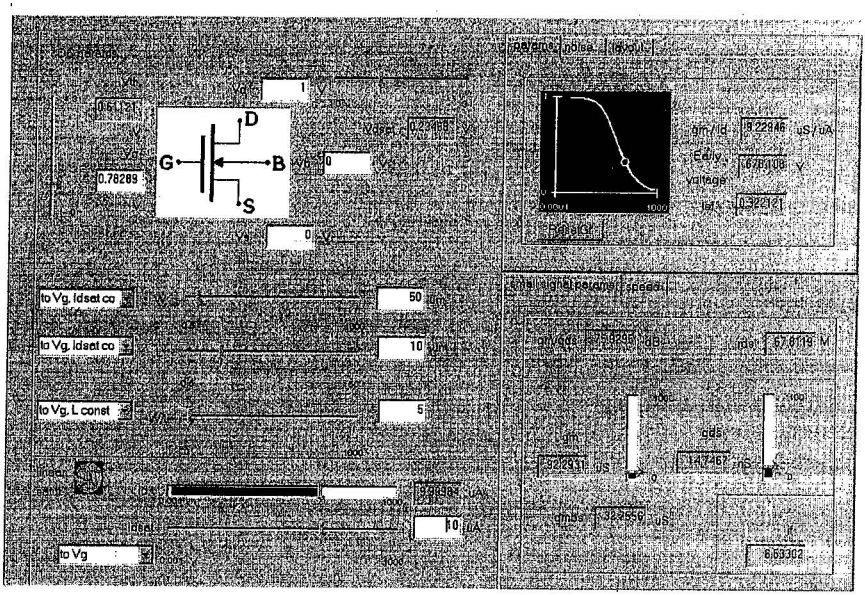

Figure 2. The user interface for transistor cell design

The structured transistor sizing consists in setting transistor priority targets (gain, noise, speed). After terminal voltages are set, there are only three variables to change: channel width W, channel length L and drain current I_D.

The proposed design procedure consists in imposing I_D and then selecting the gm/I_D ratio by setting the channel length (L) and calculating the channel width W. Therefore, the freedom variable is W and it can be changed interactively to fit the circuit targets while observing all other design parameters. When the channel width is determined, this parameter can be set and the channel length can be changed as tradeoff between speed, linearity, dynamic (smaller L) and DC gain, noise (lager L).

If transistor dimensions are set, the drain current can be changed leading to change level of inversion as a trade off between speed, linearity, dynamic (strong) and DC gain, noise (weak).

The user interface for transistor cell design is shown in Figure 2. General parameters which are calculated are: gm/I_D, Early voltage U_A, transconductance efficiently factor gmU_T/I_D, equivalent noise, small signal parameters, gain, output resistance, parasitic capacitances, transient frequency and layout area.

4. Basic Analog Structures

The present version of this tool covers the following basic analog structures: differential pair, current mirror and cascode stage. For these structures we define general behavior and specific behavior. General behavior is actually transistor behavior, with the same general parameters and dependencies. Specific behavior is related to specific features and parameters which are defined for specific analog structure.

It means that every chart displays the same graphical interface, the same parameters as for transistor cell design, plus some specific structure parameters.

Therefore, the analog design procedure consists in:

- setting priority targets (speed, area, noise, etc.)
- setting bias current
- setting g_m/I_D ratio according to circuit level specification
- changing interactively W or L to adjust level of inversion, if needed. And watch, all the time, all other parameters!

4.1. Current mirror

In the initialization step of the current mirror, the bias current has to be defined. The design procedure consists in setting L (for an imposed current value) and changing W to get the best other parameters' values.

Specific parameters are the current mismatch, the output resistance of the current mirror and the parasitic capacitances at the gate and drain of transistors (important for speed and stability).

4.2. Differential Pair

Differential pair is set to be in the saturation region, which has to be the mode of operation of this structure. For an initial current value, the ratio W/L will be proposed, and moderate inversion of operation. The design procedure consists in setting L (for an imposed current value) and changing W to get the best other parameters' values.

Specific parameter is the voltage mismatch which influences the total offset voltage of the circuit with the differential pair as input.

4.3. Cascode Stage

In the initialisation step of the cascode stage, the input voltage and the drain current have to be defined. Using these conditions, the ratio W/L of the input transistor is proposed, and the voltage U_{bias} for the cascoding transistor is calculated.

The design procedure consists in adjusting W (L) of both transistors with respect to the other parameters. For every change, a new value of U_{bias} is calculated.

Specific parameters are the output resistance, the gain and the input capacitance of the cascode stage.

5. CONCLUSION

In this paper a new chart oriented CAD tool for CMOS transistor and basic analog structure sizing was presented. Charts are very useful whenever the user is asked to make a choice. This tool is dedicated to help analog designers to make optimum design choices over full range of inversion level inversion level (weak, moderate, strong) of MOS transistor.

6. REFERENCES

[1] D. Glozić, V. Litovski, and R. Bayford, "ASCOTA3 - A New Automatic Hierarchical CMOS Opamp Synthesizer", Facta Universitatis, series: Electronics and Energetics, Vol. 4, No. 1, 1991, pp. 81-105.

[2] D. Glozić, V. Litovski, and R. Bayford, "ASCOTA3 ADIL: A New Reconfigurable CMOS Analogue VLSI Design Framework", Microelectronics Journal, Vol. 25, No. 5, Aug. 1994, pp. 335-351.

[3] C. Enz F. Krummenacher and E. A. Vittoz, "An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications", J. Analog Integrated Circuits and Signal Processing, Vol. 8, July 1995, pp. 83-114.

[4] M. Bucher, C. Lallement, C. Enz, F. Théodoloz and F. Krummenacher, "The EPFL-EKV MOSFET Model Equations for simulation, Version 2.6" Technical Report, EPFL, July 1998, available on-line: http://legwww.epfl.ch/EKV

[5] R. Spence, "The facilitation of insight for analog design", IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Vol.: 46, No. 5, May 1999, pp. 540-548

[6] D. Binkley, M. Bucher, D. Foty, "Design-oriented characterisation of CMOS over continuum of inversion level and channel length" , The 7th IEEE International Conference on Electronics, Circuits and Systems, 2000. ICECS 2000. Vol. 1, 2000, pp. 161-164.

[7] F. Silveira, D. Flandre, P. Jespers, "A gm/Id based methodology for synthesis of CMOS analog circuits and its application to the synthesis of a Silicon-on-Insulator micropower OTA", IEEE Journal of Solid-State Circuits, Vol. 31, 1996, pp. 1314-1319.