Microprocessor module with a programmable address decoder

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The role of microprocessor modules as building blocks of external expansion bus-module systems (BMS) is often discussed in technical literature. Enormous amount of such modules is developed and supplied by individual firms, institutes, etc. The evolution of contemporary technology and element base provide the opportunity for continuously increasing the requirements concerning these modules, which consequently integrate more and more system resources and offer alternative system preconfiguration.

Regardless of the quick progress of 16- and 32-bit microprocessor orientated multiprocessor BMS, a pleiad of bus-module controllers from various suppliers evidence that the niche destined for smaller system configurations still remains unoccupied.

The requirements concerning microprocessor modules forming small BMS can be restricted :

* Support local microprocessor bus for future system expansion;
* Eventual quick and flexible preconfiguration of system resources;
* Guarantee for a fast reception and servicing and processing of priority interrupt requests without delay;
* To include control devices to monitor normal system functioning;
* To include power supply supervision controllers which guarantee preservation of current system status in case of supply malfunctioning;
* Support of time-clock and a calendar;
* Multifunction input/ output connection system for linking a variety of peripheral set-up;
* To offer a possibility to join a local industrial computer net.

To comply with these requirements we developed a model based on the MC68HC11 microcontroller IC and the multifunction input/output device GM3004C of Goldstar. The latter includes: 2 serial communication adapters, software compatible with UART NS16C450; bi-directional parallel CENTRONIX port; floppy-disc supervision controller, software compatible with the 82C765B industrial standard. A build-in decoder follows the state of 9 address lines - in this case the resources location in the 512-byte address space corresponds to the address allocation of respective devices in the input/ output field established in the IBM/PC AT personal computers.

Supply voltage monitoring and support of real-time clock and calendar is realized by means of a specialized IC MC68HC68T1.

On Figure 1 is shown a general structural schematics of the microprocessor module.

Structural Schematics

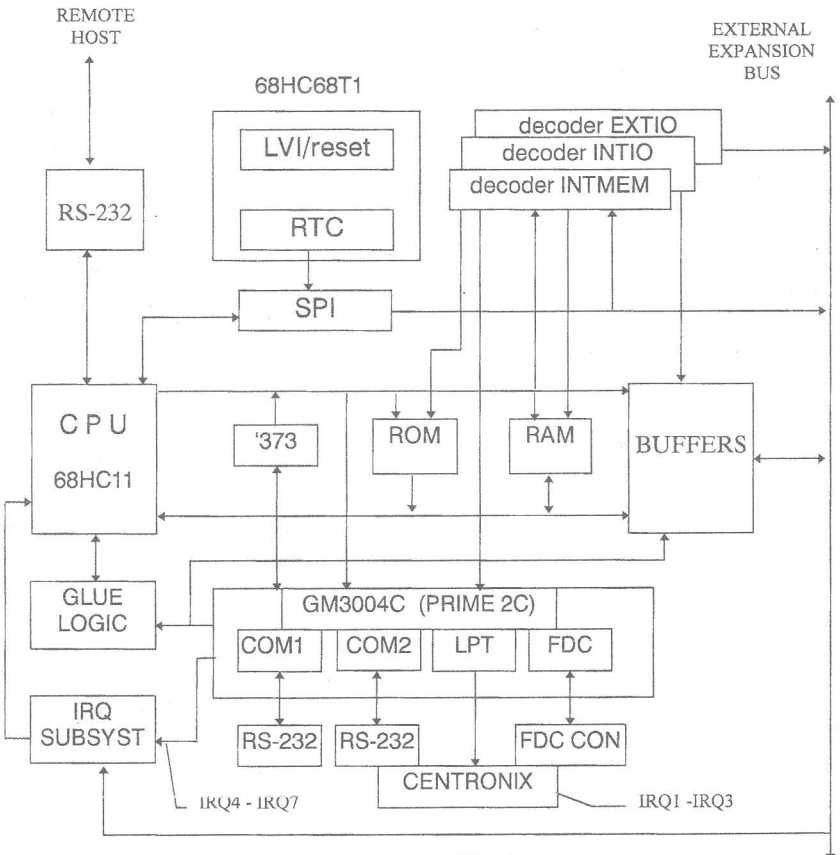


Fig.1

Different components ensure fulfilment of the above mentioned requirements concerning the module, as well as provision of necessary maintenance and control functions of the built-in bus resources.

Special attention is payed to the requirement concerning easy and quick [p]reconfiguring of system resources. The system analysis suggests that there could be differentiated 5 groups of system resources placed in a common address field:

1) RAM, EEPROM and input/output devices in the microcontroller;

2) input/output devices in the microprocessor module;

3) bus controlled input/output devices with access after decoding in microcontroller module;

4) devices with access after full decoding done in peripheral modules, with send back block decode signal;

5) ROM and RAM placed in the microprocessor module. The requirement for easy redistribution of these zones in the common address space imposes either building-in a memory control system device or creation of a programmable address decoder. The second approach is used because it appears as a natural extension of the basic concept for intrinsic resources control of the MC68HC11 microcontroller.

On figure 2 is shown the principal electrical scheme of the address decoder. The 74HC164 shift register there is placed untraditionally. After the initial settling SR is resetted. Configuration data byte (includes BASEIO 6 bits plus 1 bit contol info) from the serial peripheral interface (SPI-MOSI line) of the microcontroller enter its serial port. Also the clock train SCK from SPI passes through the closed analogue switch K1 towards SR's clock input port.

In the same time K2 is in the OFF state and blocks the interchange with other devices (e.g. MC68HC6T1) connected with SPI. In this way it is possible to expand the system initialization procedure in order to include a base address(BASEIO) settling. BASEIO controls the activation of on-board input/output devices via INTIO signal and activation of decoded external bus zones via EXTIO signal.

The leading bit of the 8-bit word, set up in the register, is obligatorily set to 1 which results in changing K1 to the OFF state and closes K2. In this way the register blocks itself, while the clock sequence SCK passes to the other devices connected to SPI.

The least significant 6 bits (BASEIO selection) of the SR word are compared with current address of the high priority address lines. In case of coincidence U12 forms BASEIO signal to enable INTIO (U13A) and EXTIO (U13B, U14A) generation circuit and to disable INTMEM selection circuit (U14B). If the decoder U13A is enabled then works out 2 control signals, IOR* and IOW*, responsible for the interchange with the multifunctional GM3004C integrated circuit. The built-in decoder in GM3004C places the inner I/O registers in the upper 512 bytes of the currently decoded 1024 bytes zone.

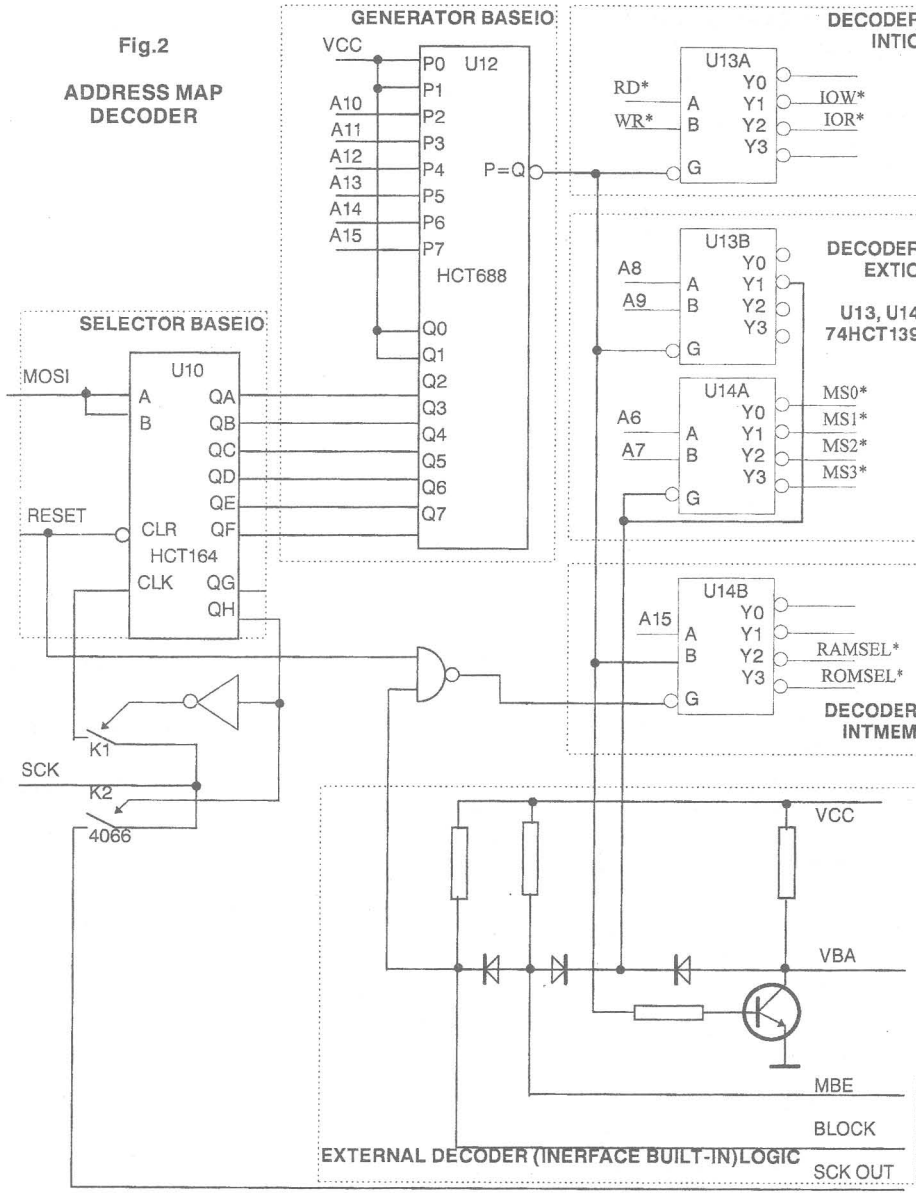
The field, corresponding to the external expansion I/O devices (EXTIO zone), is decoded by U13B and U14A and is divided into 4 zones with 64 bytes each (MS0 - MS3). The signals formed in this way pass to the system bus in order to be made a selection between peripheral ICs in other modules.

Throughout the time corresponding to selection of EXTIO address segment, is prohibited the action of the U14B decoder which divides the address field into 2 zones - for RAM and ROM.

This decoder is also blocked when a BLOCK signal comes from the external system bus. This takes place when a full address decoder in a peripheral module deciphers its valid address passed by means of the address bus. The decoder is realized in this way because it is possible one

Fig.2

ADDRESS MAP DECODER



and the same "physical" address to be decoded by different devices. The resources access priority system used excludes any possibilities for arising conflictsituations. Except that, the approved priority order is as follows:

1) inner RAM, EEPROM and input/output devices of the microcontroller; 2) internal registers of GM3004C and 4 preliminary decoded bus zones; 3) bus modules for full decoding of "physical" addresses and supporting BLOCK signals; and in the end - 4) with the lowest priority are the system RAM and ROM. This system decoder organization gives unlimited freedom to complete and configure systems.

Basic microprocessor module characteristics:

- ROM and RAM - 32 kbytes each;
- system bus for configuration extention;
- real-time clock/ caledar;
- RS232C serial channel interface to system console;
- power supply monitoring system (Low Voltage Inhibit);
- 8-channel 8-bit analogue to digital converter;
- 2 serial assynchronous communication channels;
- parallel input/output channel for printer control;
- 2 floppy discs control interface;
- power consumption in active mode - less than 40 mA;
- battery consumption when lacking a power supply - less than 14 μA.

These basic characteristics furnish several specific alternatives:

- long-time work with battery supply only;
- multichannel analogue information inputs;
- accumulation and compression of input information into great massives for a very long time;
- quick transmission of accumulated data through 2 high-speed serial channels from 9 up to 56 kbit/s);
- drawing out accumulated data by means of a built-in disc subsystem and consequent off-line processing by the workstation.

The technical characteristics and specific alternatives of the microprocessor module define the application area. For example:

- building automatic appliances for continuous registering of temperature, humidity, pressure, etc.;
- monitoring subsystems for long-term scan of great guard systems;
- portable multichannel slow-scan osciloscopes;
- selfrecording automatic tachometers for automotive industry;
- systems for long-term recording of biological signals in medicine.

References:

1. Floppy disc controller with dual UARTs, PIO, GAME and IDE interface. Application circuit of PRIME 2C for AT - LG Semicon Co. Ltd. July 1993.

2. MC68HC11. Reference manual - Mototrola Inc, USA, 1990.

3. The 8086 IBM PC, PS and Compatibles, Assembly Language, Design and Interfacig; Vols I and II - Mazidi M. A., J. G. Mazidi, Prentice Hall Inc., New Jersey, 1995.