MADE™ design kit for Cadence Design Framework II™

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Abstract: The paper aims to acquaint IC designers with the capabilities offered by Alcatel Mietec's MADE™ design kit for Cadence Design Framework II™ CAD/CAE system. Some introduction to Cadence™ and basic description of the system is given in the first chapter. An examination of specific features of the MADE™ kit is presented further. The emphasis is put on Analog schematic simulation, Abstract generation and Automatic Place&Route features.

A brief Introduction to Cadence™

The architecture of the Cadence™ systems is the basis of the user-configurable, integrated environment Design Framework II™, which provides an easy access to the various Cadence™ modules and tools. The unique Design Framework II™ architecture solves many problems traditionally associated with CAD systems, as various user interfaces control and data conversions between applications during the sequential or parallel design stages. Design Framework II™ provides a common-look user interface to all Cadence™ integrated tools. Each tool works concurrently and shares the data flow streams of the other tools without having to do tedious data conversions. Design Framework II™ environment provides this feature transparently to the user. The following *features* of Cadence™ make the best of it.

- Hardware compatibility - allows to run Cadence™ software on DEC, HP, IBM и SUN work stations.
- Versatile Graphics Interface based on industry-standard Motif™, Open Look™ or Oliver™ Window managers - makes it easy-to-learn CAD system.
- Unified Data Base (UDB) eliminates tedious data conversion and allows several integrated tools to use the UDB concurrently providing even temporary data results to the rest of applications.
- Modular, configurable, high-capability environment. New tools and applications can be integrated into the Design Framework II™, taking advantage of the UDB.
- using SKILL™ functions in SKILL-function subroutines or from the command line.

- Menu-driven. Many of the SKILL-function routines are linked to drop-down-window menus freeing the designer from having to learn the SKILL-function language programming.
- Common project coordination and protection. Design projects are protected by check-in/check-out procedures. Several projects can be edited and several designers can work on the same project. Privilege access is coordinated at Cadence™ level in addition to UNIX level protection.

When discussing specific Cadence™ features for project maintenance and control a few words on *terminology* should be introduced. The design project is identified with the project library. The project library comprises of cells, which have various view presentations and thus a cell-view is formed. This is a logical presentation rather than a physical object. The Internal Design Manager supports links to physical data files in a way that design data files are managed transparently to the user which is one of the worthy features of Cadence™. It is worth to mention that Cadence™ allows well-equipped users to manage data at a file level using SKILL™ language of the system. SKILL functions, which are very much 'C'-like build the core of the system and represent the lowest level of the user interface. The most of Cadence™ itself has been developed using these system calls and 'C' code.

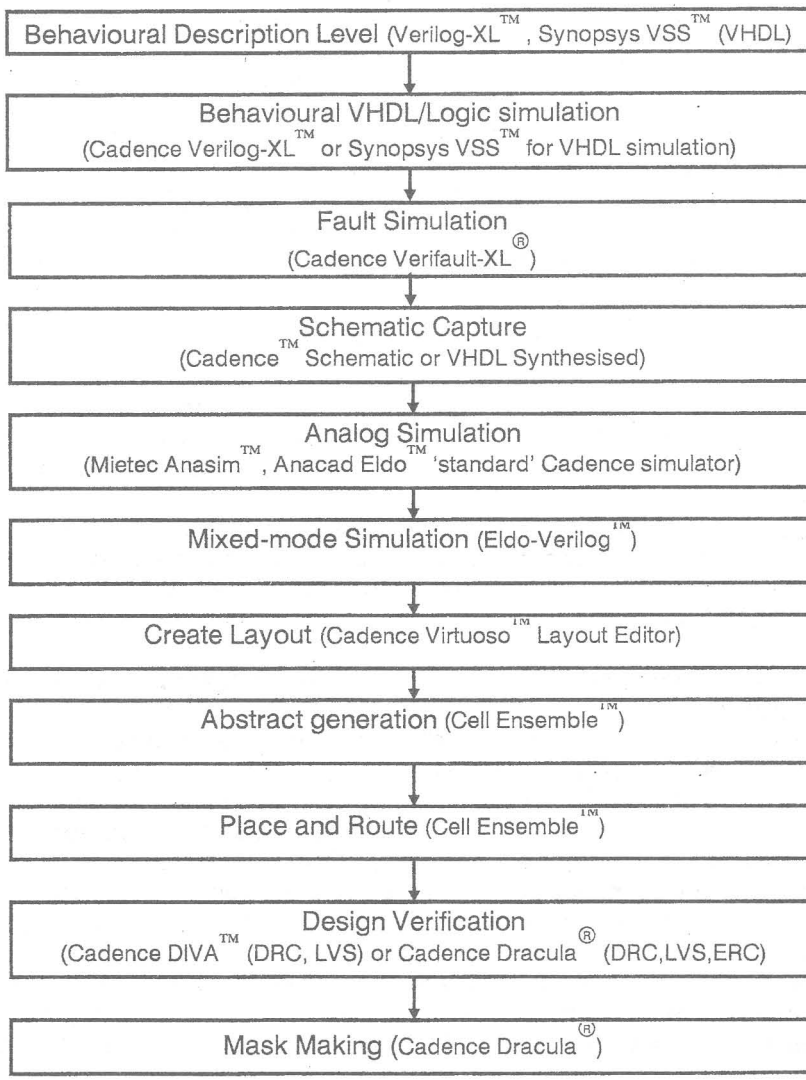
Another valuable feature of Cadence™ is easily accessible *Design Hierarchy*, which provides multiple-level design data and conforms with the „Top-Down" concept perfectly. This lets simulations at each level - behavioural, schematic, post-layout concurrently and almost independent to how complete is the whole design.

Technology data is preserved in a so-called *technology file*. This file contains various definitions concerning layers, devices, design and extraction rules. The technology file is human-readable and even though it provides a transparent technology concept, well-equipped designers can edit the file.

MADE™ design-kit as an illustration to Design Framework II™ environment.

Cadence™ is built as an „open", "modular" and „technology adaptable" system under a unified user interface. *The technology mobility* is supported by the so-called *design kit*. The design kit for the specific technology comprises of a set of technology data files, standard cell libraries, semi-custom cell libraries, files containing SKILL™ routines, specific tools or modules, device model files at assorted model levels , model parameters files and etc. - all the necessary technology-dependant data. *Switching between technologies* is often as easy as running the software using another environment set of initialisation and technology files. In view of design data conversion, there are many developed built-in translators to import and export design data in a variety of 'industry standard' formats - CIF, LEF, DEF etc.

MADE™ stands for 'Mietec's Analog and Digital Engineering system and optionally uses CMOS as well as HBiMOS Mietec technology. The kit includes standard and semi-custom cell libraries, modular technology file and CAD tools by well-known CAD vendors. A brief summary of the kit contents will be presented by illustration of the „Top-Down" design concept. Capabilities are typical for Cadence™ as a whole, but the specific tools may differ from kit to kit.



In addition, there are tools available for:
- Logic Synthesis - Synopsys™ HDL & VHDL design compiler
- Test Synthesis - Synopsys™ Test Compiler
- Switched-Capacitor systems - Mentor™ Autofilter

This design scheme is known as „Front End Design" and is pre-determined by the software launch. The alternative design scheme is „Back End Design" and depicts design from the lowest (layout) level to upper representation levels.

Not the whole of the described full tool frame is essential to the system, the minimum tool set can comprise of only a few tools for Logic simulation, Analog simulation and Waveform Processor. This reveals the modular feature of Cadence™. *The core of Design Framework II™ system* is also „open" for access by the built-in *SKILL™ function interpreter.* For instance, MADE™ kit includes an extensive set of SKILL™ function routines which, in some cases drastically change the typical Cadence™ menu-driven design flow dialogue. This is a MADE™-specific feature which in spite of the disadvantages in user-interface uniformity illustrates the capability of Cadence™ to adopt various externally-developed CAD systems and emerges Cadence™ expandable concept.

MADE™-specific design flow control features for Analog simulation, Abstract generation and Place-and-Route procedures.

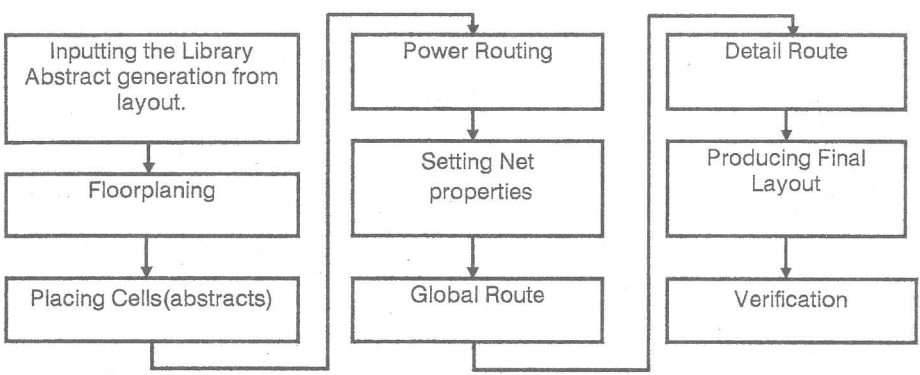
Analog Simulation in MADE™ is carried out by the Mietec's analog simulator ANASIM™ which is a kit-specific tool, not usually present in Cadence™ tool frame. Optionally, the kit can use Anacad Eldo™, which is far much better in CMOS analog simulation and device modelling. Anasim is a SPICE2™ G6 Berkeley based simulator with built-in device models. User can only specify the necessary model parameters, otherwise the default parameters will be used. Depending on the model parameters specified the simulator switches from Gummel-Poon (default MOS model) down to a simpler Ebers-Moll model. In either case, charge storage effects, ohmic resistances, and a current-dependent output conductance may be included. The JFET model is based on the FET model of Shihman and Hodges. Three-level MOSFET models are implemented; MOS1 is described by a square-law I-V characteristic, MOS2 is an analytical model while MOS3 is a semi-empirical model. Both latter models include second-order effects such as channel length modulation, sub-threshold conduction, scattering limited velocity saturation, small-size effects and charge-controlled capacitances.

Some more details on simulation flow control can be found in „Brief Mietec's MADE™ manual (internal use)" by M.Milev, here only the *specific analog-simulation features* will be noted: graphic net-list error display, variables versa parameter values, graphic simulation error display (small-signal linearity violations, model mode violations and etc.). It has to be noted that MADE™ kit

uses Waveform™ simulation results display processor rather than the Cadence™ built-in cWaves™. It offers some new features as band-width calculation, 3db point extraction, phase-margin and gain-margin extraction in OpAmp simulations, but the Signal Calculator of cWaves™ is not available and its valuable 'special functions' feature is disregarded.

Abstract generation for Place-and-Route. The abstract is a high-level representation of the layout cell. It's a complete black-box view of the cell which incorporates all the necessary data for the Placer and the Router: position of pins, obstructions on routing layers, access direction of pins, conditional vias, and general geometries. The design flow control is found in [2] again. Abstract generator is part of the Cell Ensemble™ tool for Automatic or Interactive Place and Route. *MADE™ specific features* include: automatic boundary generation, automatic pin and conditional vias generation, automatic jumper-pins generation.

Place and Route. Place and Route procedures are performed by the Cell Ensemble™ tool, which is a typical Cadence™ tool. It allows fully automatic as well as interactive partial Place and Route. Procedures may vary from case to case, but typically includes the following *design flow stages:*



The Floorplaning at block level automatically estimates chip core area, creates initial placement regions and creates initial I/O frame surrounding the core. *Cell Placement* includes I/O cell placement and improvement, core cell placement either in fully automatic or designer-interactive way, allowing for placement regions editing and pre-placement regions creation.

Create Channels procedure follows. Here, there are options to find the best cut-lines partitioning and channels formation. The channel formation is not fixed and could be changed during the following steps of Global routing and Detailed routing.

Global Routing allows setting the net properties, net priorities, congestion cost estimation and reassigning nets from channels with higher congestion cost to channel with lower congestion. *Global Routing Algorithms implemented are*:

expansion routing - for most typical signal nets; tree routing - to route nets which have pins spread over the entire design, such as power and clock; and enhanced tree routing which has less constraints than the routing tree algorithm.

Detailed routing is a gridless routing that creates physical routing geometries to connect the logical connections assigned in the channels by the global router. The detailed router routes all nets, including power and ground. When the detailed router finishes routing a channel, it compacts or expands the channel in order to accommodate more nets or to save space. It can move rows and blocks adjacent to the channel to adjust the size of the channel and to save core space.

Options vary from fully automatic routing to manual physical routing. There are several optimisation options as well. Design flow commands for Place and Route are given briefly again in [2].

In conclusion *Other MADE™ features* will be listed, which are not discussed in this paper.

- *Design Import and Export* from/to Synopsys™ or Synopsys/Verilog™ in addition to Cadence™ typical translators to/from physical EDIF, CIF, CALMP, DEF formats as well as CDL, TEGAS, SICOS, SDL netlist formats.
- *Layout Compiler* for regular layout structures (in CMOS 0.7 technology) - Static one- and dual-port RAM, Static synchronous ROM, Static asynchronous FIFO, digital Multiplier.
- *Bonding Diagram Editor*.
- *Delay Calculator* (logic and mixed-mode pre-layout simulation of signal parasitic delays)
- *Post-layout Extraction of Parasitic capacitances* and re-simulation.

Summary Notes:

This paper summarises IC design experience output accumulated at ECAD Laboratory, Technical University-Sofia using Cadense™ and Alcatel Mietec 2u CMOS and 2u HBiMOS design kits.

Bibliography:

[1] „9401 Cadence™ on-line library", Cadence Design Systems, Inc. 1992
[2] „Brief Mietec's MADE™ manual (internal use)", Momchil Milev, 1996
[3] „Abstract Editor - MADE™ internal user guide", Alcatel Mietec, 1995
[4] „Cell Ensemble - MADE™ internal user guide", Alcatel Mietec, 1995