HAZARDS IN DIGITAL CIRCUITS AND ITS MODELING WITH PSPICE

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ABSTRACT: The real gates are characterized by a finite propagation delay whose presence may lead to the appearance of some short false pulses in the case of logic circuits or to the delay depending of the evolution in the case of sequential circuits. Such situation must be pointed out even in the designed phase of the circuit to be able to take measures for a correct functioning of the circuits irrespective of the propagation delay. The theoretical analysis, because of the difficulties that appear, is generally made on simplified models. The PSpice program allows of the more complex analysis of the circuits that will allow much better understanding of the phenomenon and the efficient elimination of the undesired effects.

Introduction

One of the most difficult concepts to explain within the course of digital circuits, is that of hazards. As is known, hazard is due to propagation delay of the signals through logical devices, and its presence may compromise the correct functioning of the circuits. The mastering of the phenomenon, both from a theoretical and practical point of view, is essential for a designing engineer.

In the speciality literature there are to be found complex theoretical analyses of the hazard in the digital circuits, which are not always easy to follow and to understand. The existence of PSpice programs, even in its evaluation version, allows the hazard modeling that may lead to a better understanding of the theoretical aspects.

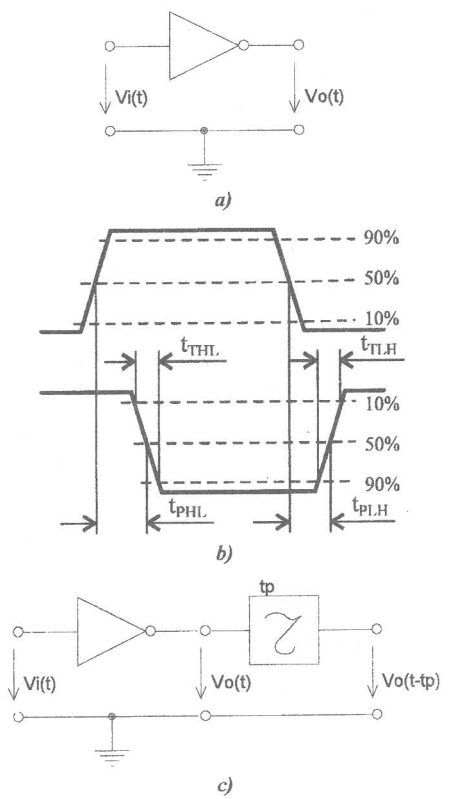

Figure 1 a) Real inverter b) Transition time and propagation delay c) Simplified model for real inverter

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Transition time and propagation delay

For one inverter the transition times and propagation delays are presented in *Figure 1*. The above mentioned times vary from one example to another. In the device catalogue there are generally mentioned the typical values as well as the minimum and maximum ones.

The transition and propagation delay also depends on the change of direction ($t_{PHL} \neq t_{PLH}$, $t_{THL} \neq t_{TLH}$) and in the case of the gates with several entrances sometimes may depend also on the entrance that changes its state.

The theoretical analyses are generally made using a simplified model of the gates from the point of view of the propagation delay. In this simplified model the real gate is replaced by an ideal gate followed by a delay element. In the model in *Figure 1.c* we consider a unique propagation delay and we neglect the transition times.

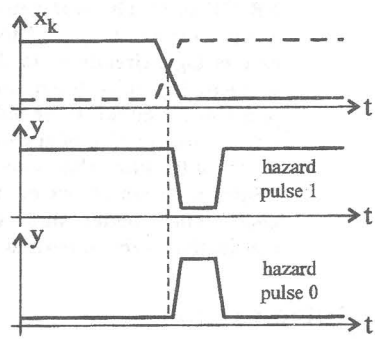


Figure 2 *Static hazard*

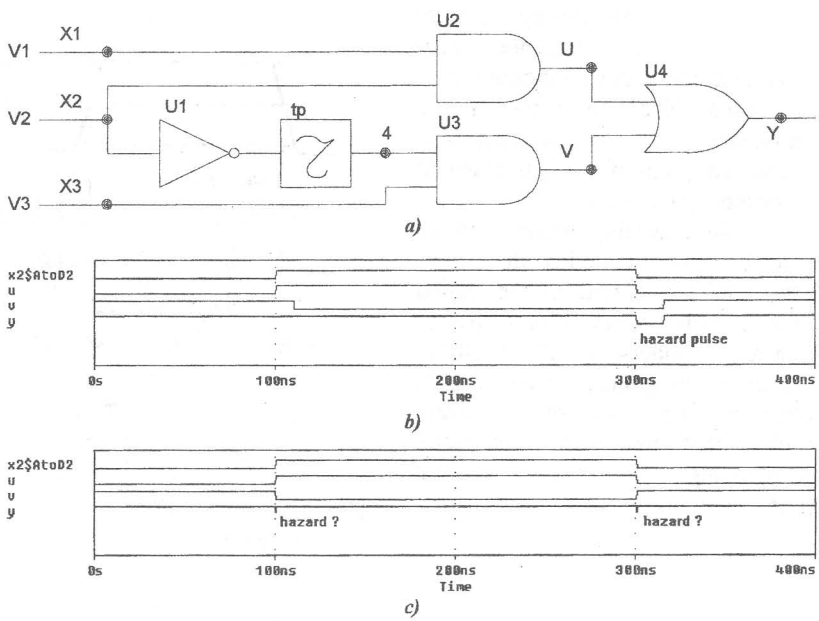


Figure 3 *a) Static hazard example b) The waveforms with real inverter c) The waveforms with ideal inverter*

Hazard in logical circuits

In a logical circuit several types of hazard situations may be identified.

Static Hazard

The static hazard is manifested by the appearance of a short pulse (a glitch of logical 1 or 0) at the output of the circuit when one of the entrance variables changes its state (*Figure 2*). This occurs although the Boolean expression of the output function shows a constant value of this. *Figure 3* illustrates this type of hazard in which only the inverter is considered a real one.

Dynamic hazard

We shall call dynamic hazard the appearance in the output signal when one input variable changes of false transition before its stabilizing at a desired value (*Figure 4*).

Figure 5 together with associated diagrams illustrates the appearance of a dynamic hazard.

The output function $Y = x_1 \cdot \overline{x_2} \cdot x_2 \vee x_2 \cdot x_3$ should present a $0 \rightarrow 1$ transition when the input x_2 varies from 0 to 1 but because of the delays

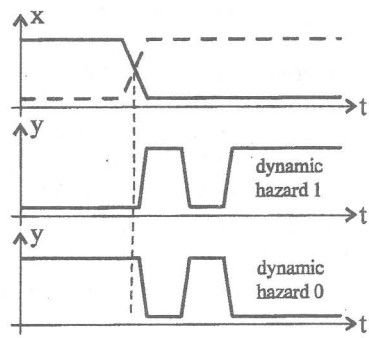


Figure 4 Dynamic hazard

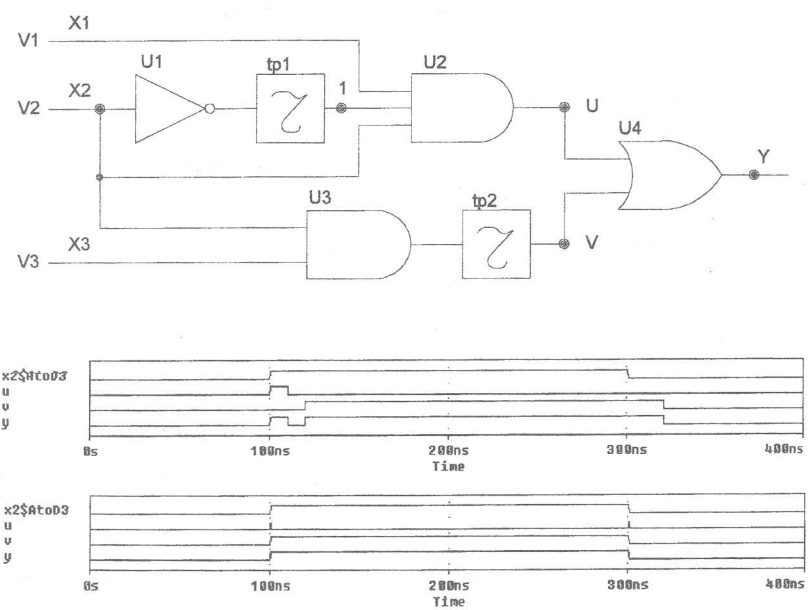


Figure 5 Dynamic hazard example

tp_1 and tp_2 this transition generates dynamic hazard. The PSpice modeling allows an analysis of the circuit depending on the relationship between tp_1 and tp_2 and stresses that dynamic hazard appears only in the case $tp_1 > tp_2$.

Functional hazard

In the above mentioned example we considered that at a given moment only one input changes its value. In fact, there are many situations in which several input variables may change simultaneously. Due to the finite delays, these will not change simultaneously, which may lead to the so called functional hazard situation.

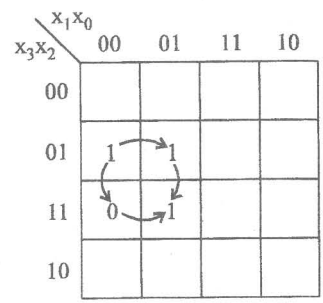


Figure 6 Functional hazard

Such an example is illustrated in *Figure 6*. The passing from 0100 state to 1101 state supposes the change of the x_3 and x_0 inputs. Depending on the value of delays after which x_3 and x_0 change, the function may pass through two possible intermediary values (1 or 0) before obtaining the final value (1).

The circuit and the diagrams that illustrate the above mentioned hazard are presented in *Figure 7*.

Note: There are situations in which the delay represents a useful element in application. Such an example is the edge detector presented in *Figure 8*, which generates an impulse both for rising and falling edge of inputs.

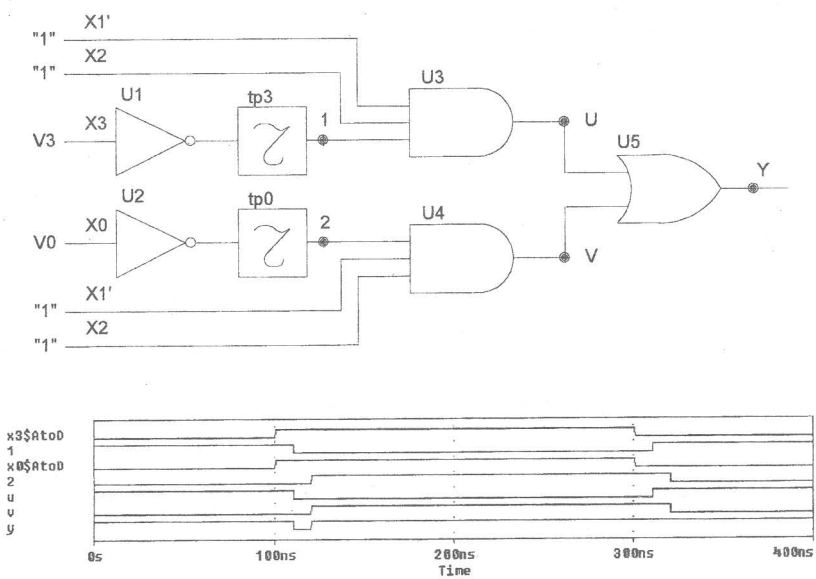


Figure 7 Functional hazard example

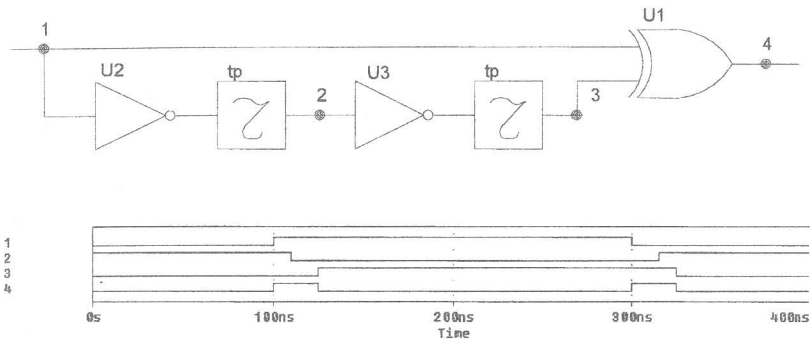


Figure 8 Edge detector

Propagation effects in asynchronous sequential circuits

A block diagram and a simplified model of the sequential circuit are presented in *Figure 9*, where we take into account only the delays on a feedback path (tp_i).

The main purpose of designing such circuits is to find such a circuit structure, which should fulfill its function properly, independent of the particular functions and the relations between the delays tp_i. To illustrate this we shall consider an easy example, the case of RS flip-flop.

The circuit functions properly as long as the inputs do not change simultaneously. In case the inputs change simultaneously, the circuit will oscillate as is shown in *Figure 10*.

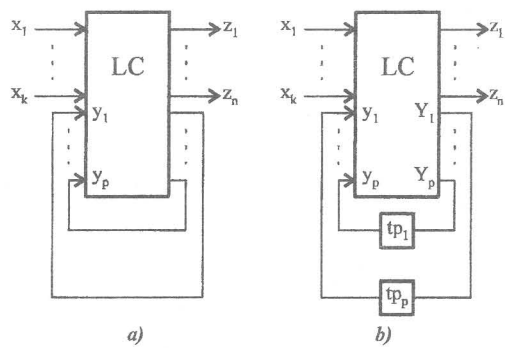


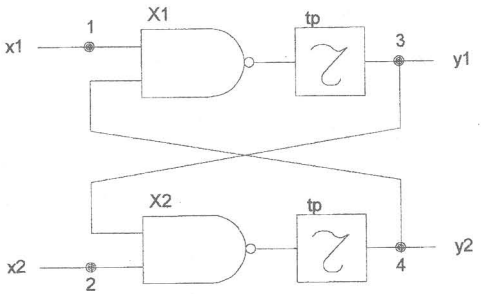
***Figure 9** Asynchronous sequential circuits*

Conclusions

To design digital circuits or systems with a proper functioning, it is necessary to make a careful analysis of the circuit even at the very beginning of the design. This avoids the possibility of the appearance of hazard situations.

In the case of complex circuits the theoretical analysis becomes extremely difficult; therefore it is recommended to use simulation programs such as PSpice.

We should also have in view that the case of connecting hazard free circuits, the resulting system itself may present hazard situations that will have to be considered and eliminated.



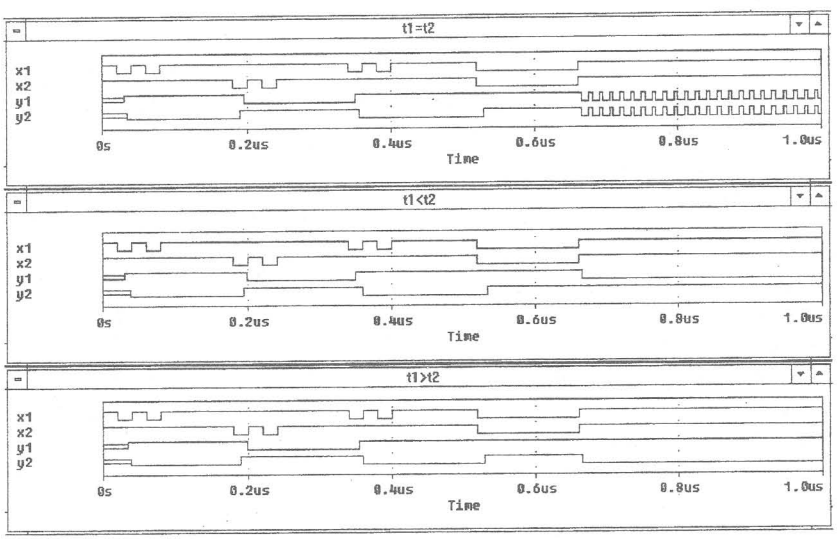


Figure 10 Hazard in asynchronous sequential circuits example

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